

Connection Block

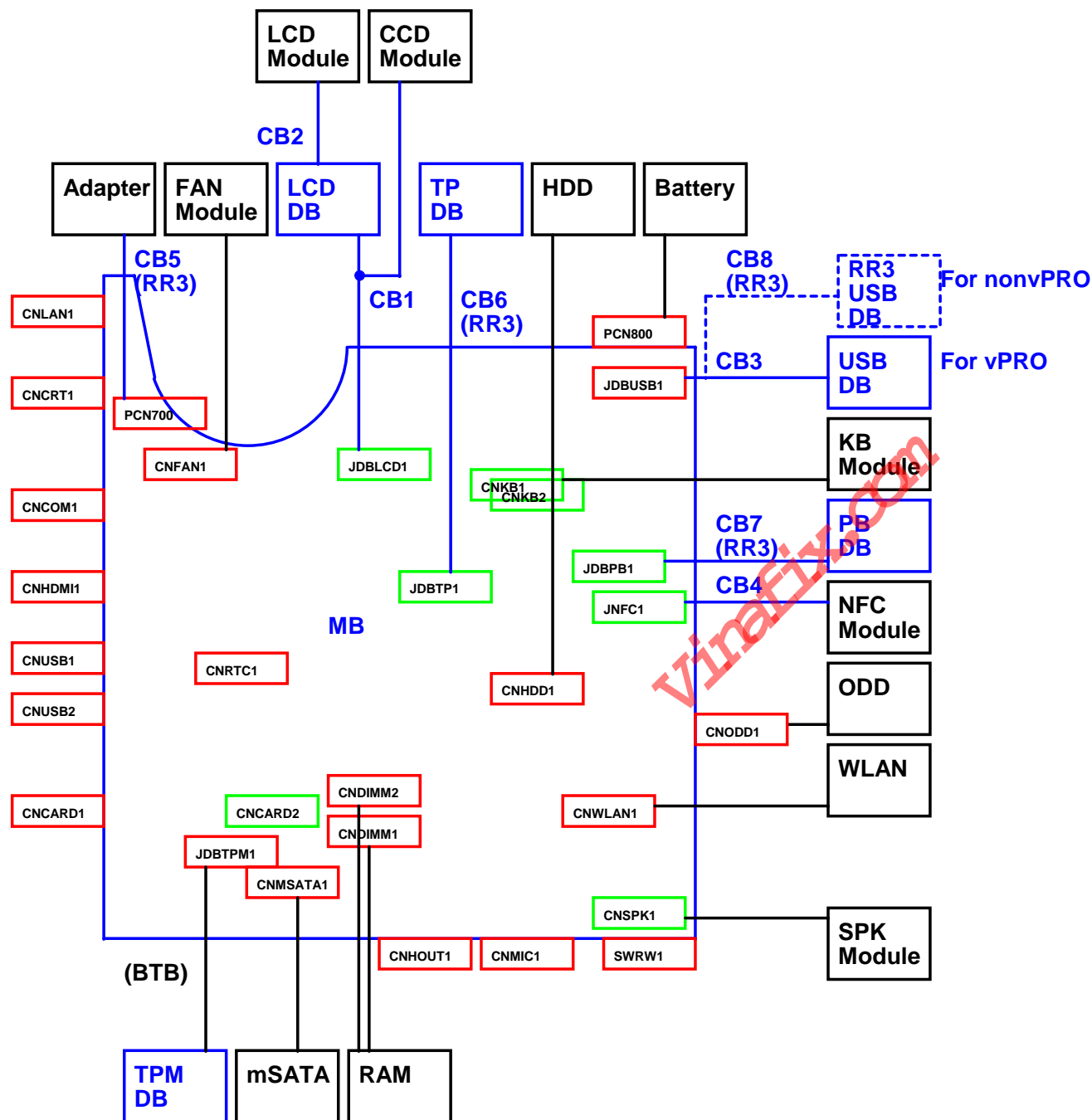


Table of Contents

PAGE	DESCRIPTION
01	Block Diagram
02	Connection Block
03	Front Page
04	Power Tree_vPRO
05	PSeq_G3 to S0 Block_vPRO
06	PSeq_G3 to S0_vPRO
07	SMBus Block&USB Table
08	CPU_HSW 1/5 (PEG/DMI/Thermal/PM)
09	CPU_HSW 2/5 (DDR3)
10	CPU_HSW 3/5 (FDI/DDI/eDP)
11	CPU_HSW 4/5 (POWER)
12	CPU_HSW 5/5 (CFG/GND)
13	PCH_LPT 1/6 (DMI/FDI/PM/VGA/DispAUX/PCI)
14	PCH_LPT 2/6 (RTC/HDA/SATA/LPC/SPI/SMB)
15	PCH_LPT 3/6 (PCIE/USB/CLK)
16	PCH_LPT 4/6 (GPIO/Thermal/PM)
17	PCH_LPT 5/6 (POWER)
18	PCH_LPT 6/6 (GND),FLASH
19	DDR3 DIMM
20	LCD CONN/NFC
21	CRT CONN/HDMI CONN
22	USB/TP/PB DB,HS/TPM CONN
23	GLAN_I217/RJ45
24	HDD/ODD/NUT
25	USB CONN
26	KB CONN/LED
27	WLAN/mSATA
28	Codec_ALC282
29	EC_NPC985
30	FAN/Serial/SIO_NCT5577D
31	CARD BUS_R5U242 1/2
32	CARD BUS_R5U242 2/2,CONN,SD CONN
33	POWER 3VPCU&5VPCU(PM6686)
34	POWER +VCC1.8
35	POWER+1.35V_SUS+/+0.675V_DDR_VTT
36	POWER +VCC_CORE (NCP81103)
37	POWER +VCC_CORE (Stage)
38	POWER +1.05V(G5602R41U)
39	POWER Thermal Protection
40	POWER AD IN/BAT IN
41	POWER CHARGER(BD8617MUV-E2)
42	Power Tree_nonvPRO
43	PSeq_G3 to S0 Block_nonvPRO
44	PSeq_G3 to S0_nonvPRO

RR3A-vPRO Power Rails

Don't support Deep Sx state
Don't support M state

Power	Voltage	S0/M0	S3/M3	S4,S5 /M3	S3/Moff	S4,S5 /Moff	Ctl Signal
+3VPCU	3.3V	V	V	V	V	V	51427ALDO5
+5VPCU	5V	V	V	V	V	V	51427ALDO5
+15VPCU	15V	V	V	V	V	V	51427ALDO5
+3V_S5	3.3V	V	V	V	V	NOTE 1	S5_ON
+5V_S5	5V	V	V	V	V	NOTE 1	S5_ON
+3V_LAN	3.3V	V	V	V	NOTE 2	NOTE 2	SLP_LAN# (NOTE3)
+3V_ME	3.3V	V	V	V			SLP_ME#
+1.35V_SUS	1.35V	V	V				SLP_S4#
+1.35V	1.35V	V					SLP_S3#
+0.675V_DDR_VTT	0.675V	V					SLP_S3#
+5V_RUN	5V	V					RUN_ON
+3V_RUN	3.3V	V					RUN_ON
+1.5V_RUN	1.5V	V					RUN_ON
+1.05V_LAN	1.05V	V	V	V	NOTE 2	NOTE 2	SLP_LAN# (NOTE3)
+1.05V_ME	1.05V	V	V	V			SLP_ME#
+1.05V	1.05V	V					+3V_RUN
+VCC_CORE	By VID	V					IMVP_VR_ON

NOTE 1: On for "Wake up function" enable during S4,S5/Moff.
Please refer to below table for brief.
And refer to DRD document for detail.

Wake Event	S4,S5 /Moff
WOL	V
RTC	V
Power Button	V

NOTE 2: On for WOL=1. Off for WOL=0

NOTE 3: SLP_LAN# could already be high before SLP_S5# and SLP_S4# (to support WOL), but will never go high later than SLP_S3# and SLP_A#

RR3A-nonvPRO Power Rails

Don't support Deep Sx state
Don't support M state

Power	Voltage	S0	S3	S4	S5	Ctl Signal
+3VPCU	3.3V	V	V	V	V	51427ALDO5
+5VPCU	5V	V	V	V	V	51427ALDO5
+15VPCU	15V	V	V	V	V	51427ALDO5
+3V_S5	3.3V	V	V	NOTE 1	NOTE 1	S5_ON
+5V_S5	5V	V	V	NOTE 1	NOTE 1	S5_ON
+3V_LAN	3.3V	V	NOTE 2	NOTE 2	NOTE 2	LAN_ON
+3V_ME	3.3V					(No use on RR3A-nonvPRO)
+1.35V_SUS	1.35V	V	V			SLP_S4#
+1.35V	1.35V	V				SLP_S3#
+0.675V_DDR_VTT	0.675V	V				SLP_S3#
+5V_RUN	5V	V				RUN_ON
+3V_RUN	3.3V	V				RUN_ON
+1.5V_RUN	1.5V	V				RUN_ON
+1.05V_LAN	1.05V					(No use on RR3A-nonvPRO)
+1.05V_ME	1.05V					(No use on RR3A-nonvPRO)
+1.05V	1.05V	V				+3V_RUN
+VCC_CORE	By VID	V				IMVP_VR_ON

NOTE 1:ON FOR WAKE UP FUNCTION ENABLE DURING S4/S5
Please refer to below table for brief.
And refer to DRD document for detail.

Wake Event	S4,S5
WOL	V
RTC	V
Power Button	V

NOTE 2:ON/OFF ACCORDING TO WOL FUNCTION SETTING

Reference data sheet

Design Guide

486713_486713_HSW_2C_Mobile_rev2_0_Final
486714 486714 HSW_2C_6L_Mob_rev2_0_Final

CPU |

487246 487246 HSW MBL EDS Vol I Rev1 6v1

PCH

486708 486708 LPT EDS Rev2 0

Check list

497750 497750 SHRKBY MBL SCH CHKLST Rev1p5

Audio

ALC282 DataSheet 0.82

Card reader

RTS5227E -datasheet

Card Bus

OZ600 -datasheet

LAN

473764 Intel® Ethernet Controller I217 Datasheet v0.96

EC |

NPCE985x 995x Rev0.3 DS Quanta

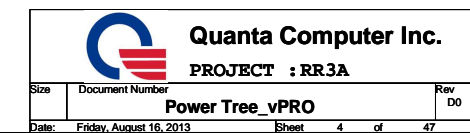
Super IO

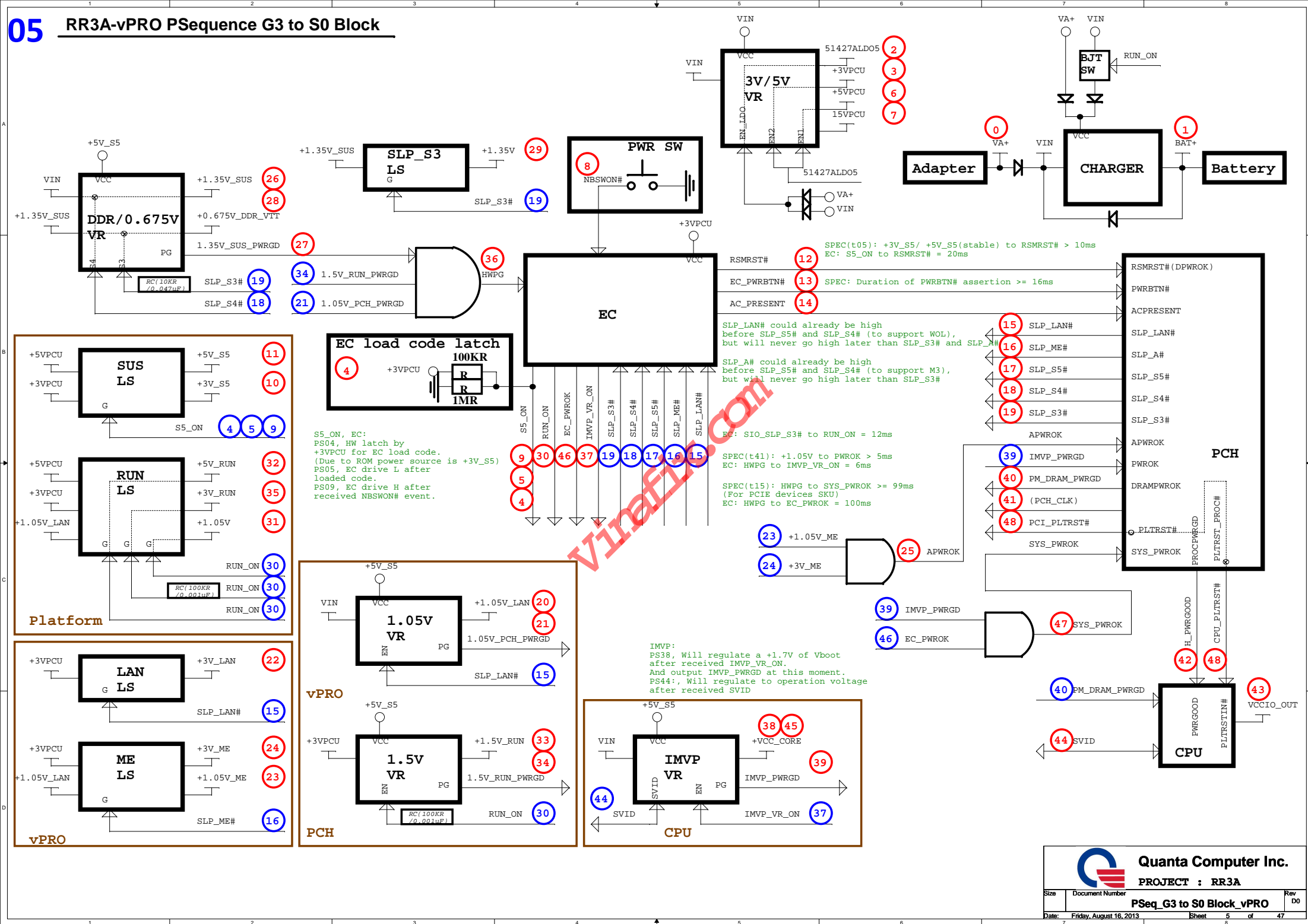
NCT5577D Datasheet V1 2

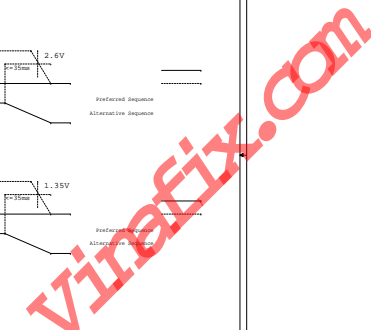
USB Re-driver

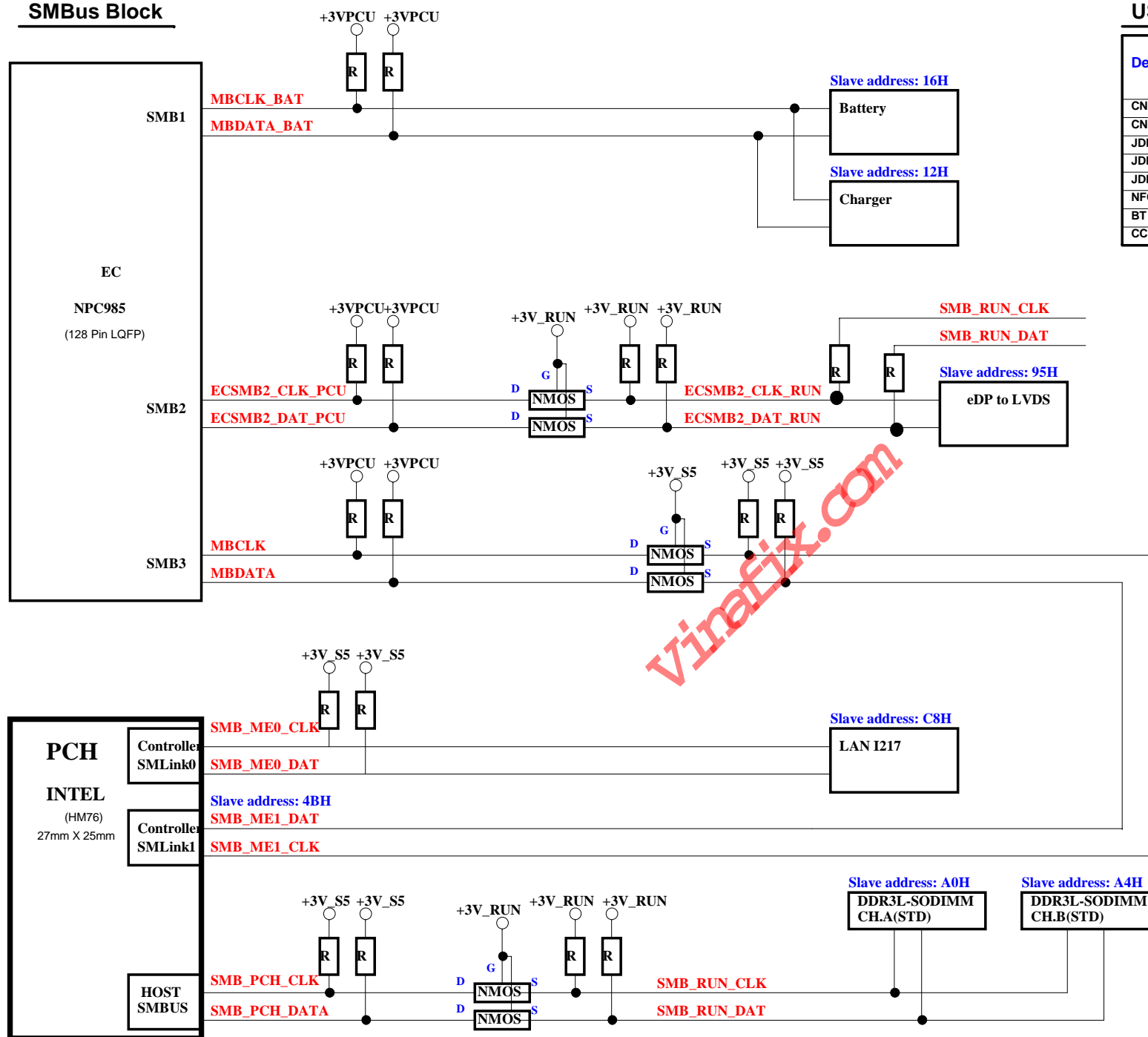
PS8713 DS Ver1.0 20120511 Quanta

RR3A-vPRO Power Tree









Device	USB2			USB3	OC#
	Pin	xHCI	EHCI		
CNUSB1	Port 1	Port 1	Port 1	Port 2	OC1#
CNUSB2	Port 0	Port 0	Port 0	Port 1	OC0#
JDBUSB1 CN1	Port 2	Port 2	Port 2	Port 3	OC2#
JDBUSB1 CN3	Port 3	Port 3	Port 3	Port 4	OC3#
JDBUSB1 CN4	Port 8	Port 4	Port 8	Port 5	OC4#
NFC	Port 9	Port 5	Port 9	NA	OC5#
BT	Port 10	Port 6	Port 10	NA	NA
CCD	Port 12	Port 10	Port 12	NA	NA



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PROJECT : RR3A

Size Document Number

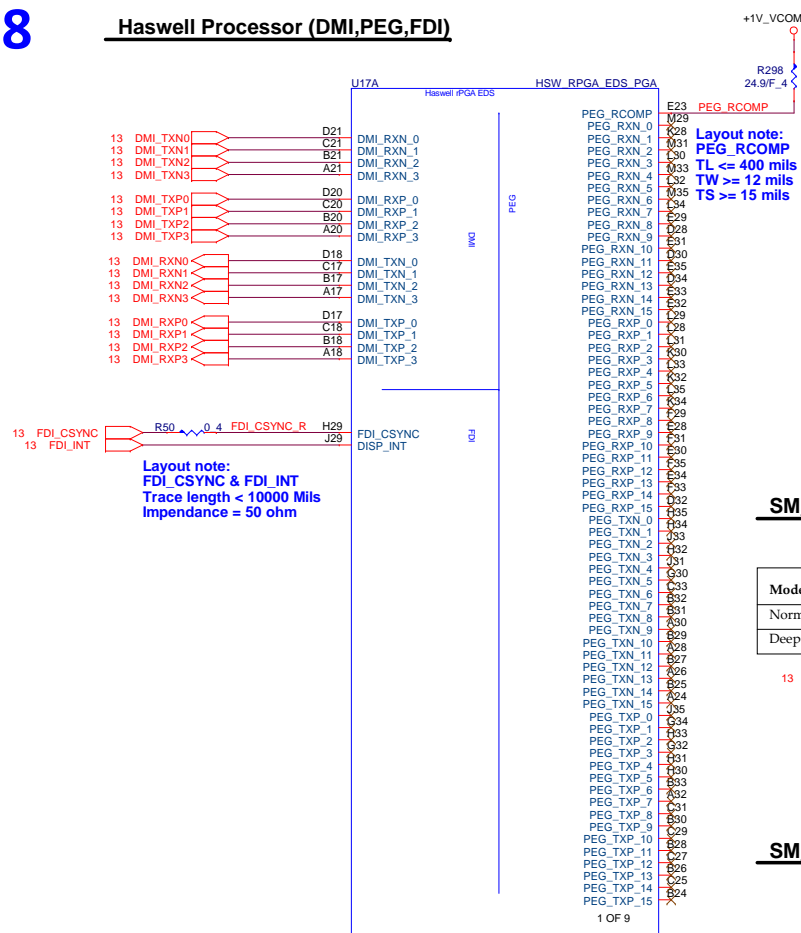
SMBus Block

Rev D0

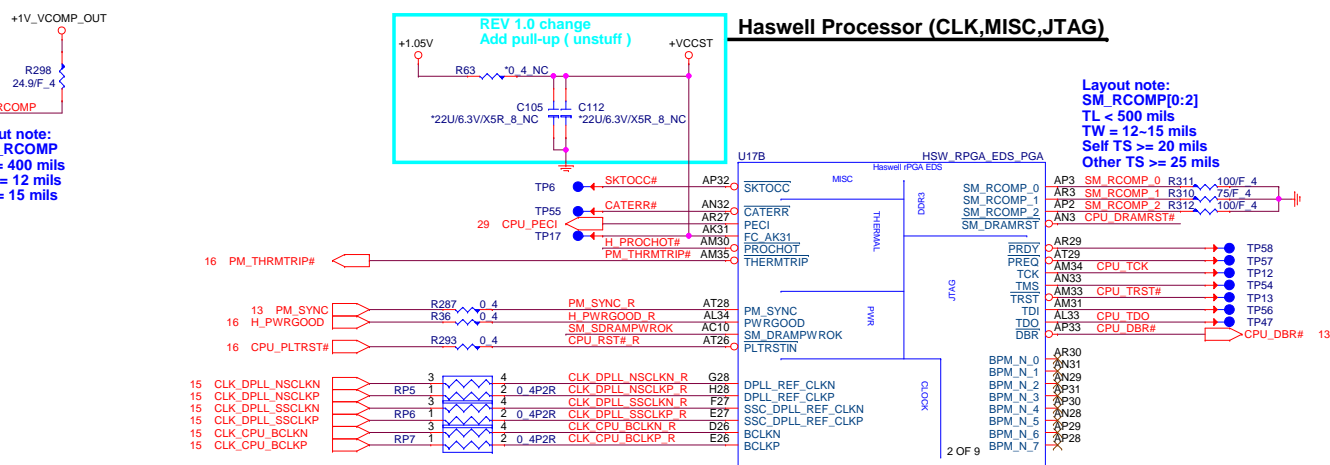
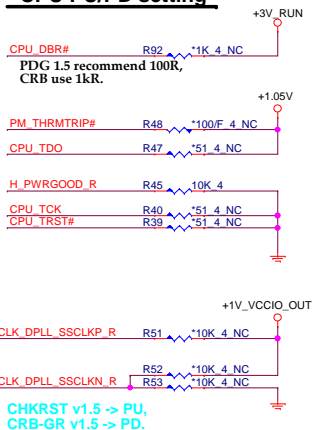
Date: Friday, August 16, 2013

Sheet 7 of 47

Haswell Processor (DMI,PEG,FDI)

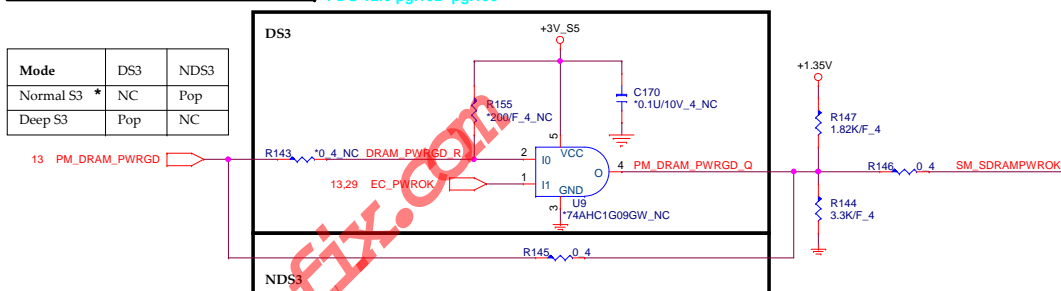


CPU PU/PD setting

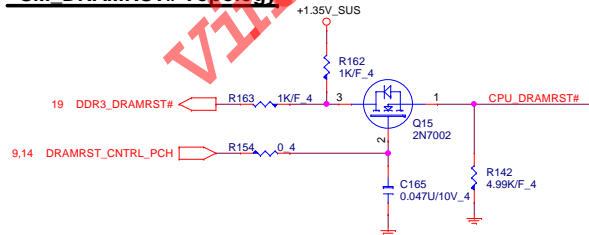


SM_DRAMPWROK# Topology PDG v2.0 pg.192~pg.193

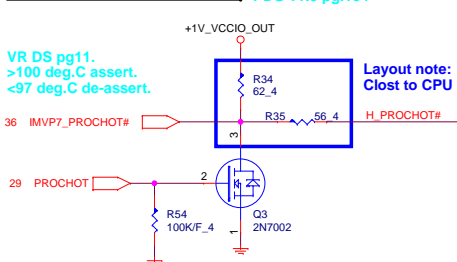
Mode	DS3	NDS3
Normal S3 *	NC	Pop
Deep S3	Pop	NC



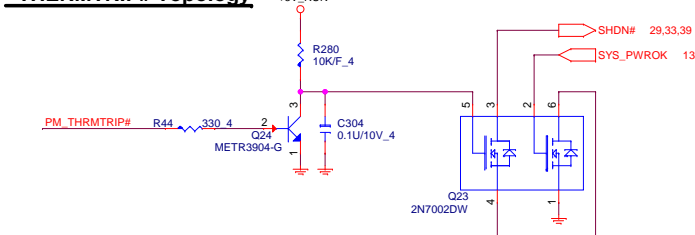
SM_DRAMRST# Topology



PROCHOT# Topology PDG v1.5 pg.184

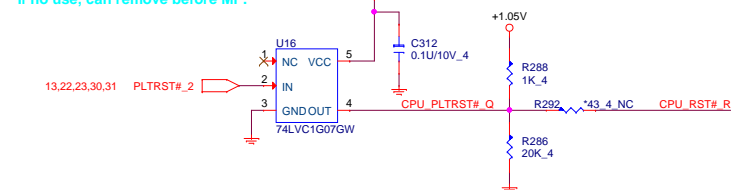


THERMTRIP# Topology

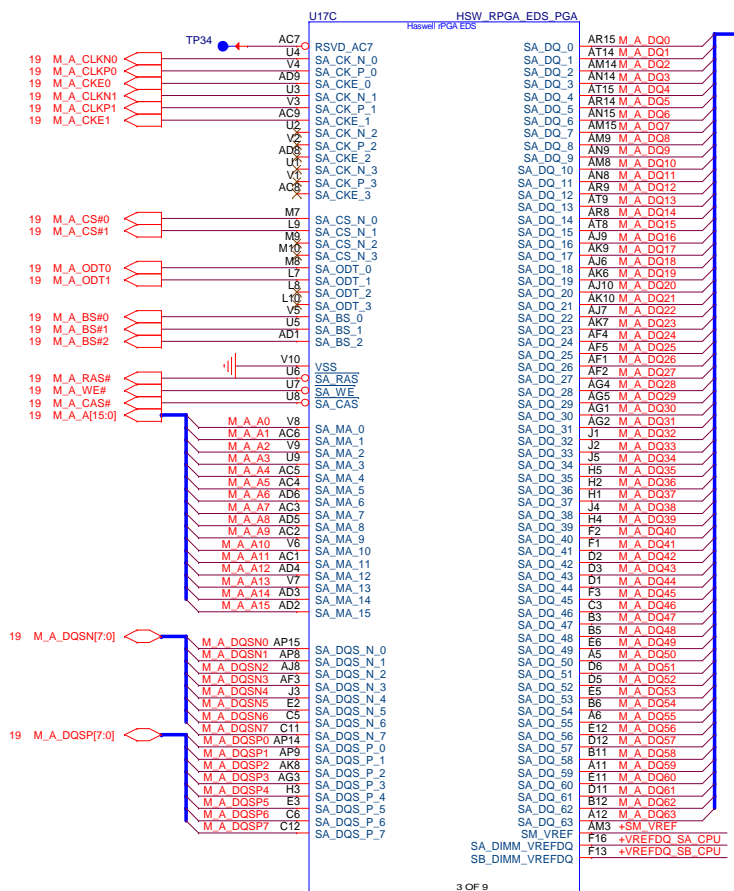


Reserved For buffer reset of PLTRSRIN#

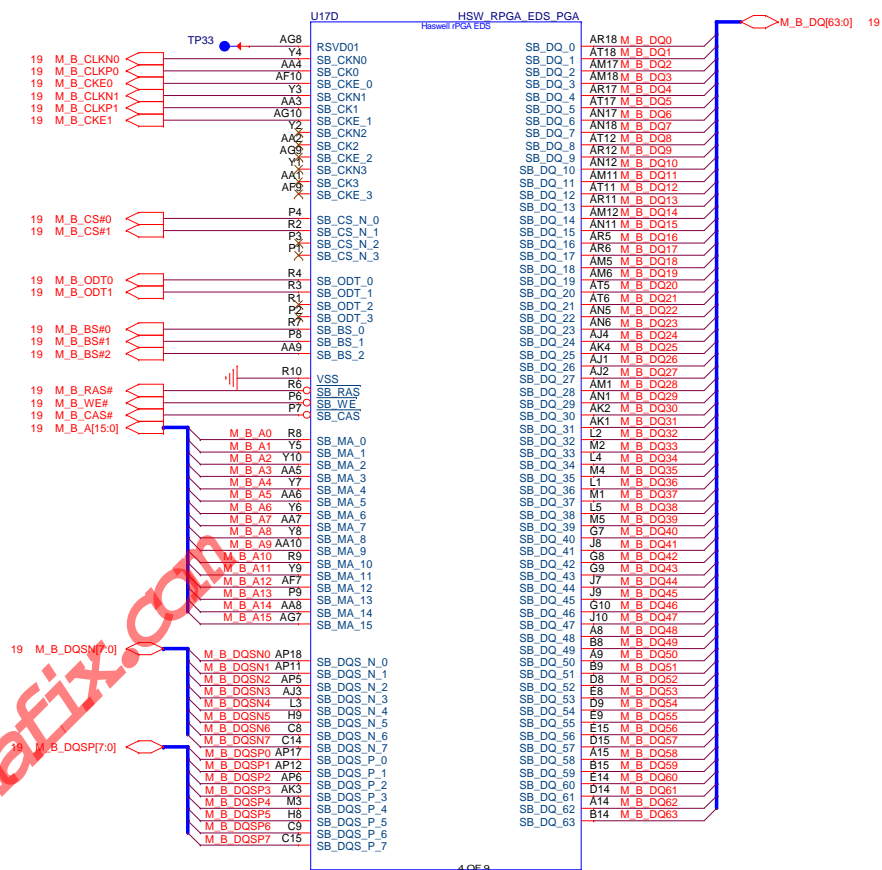
CRB-GR v1.5 pg.36
If no use, can remove before MP.



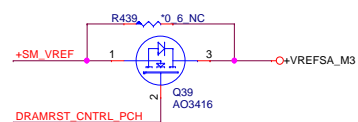
Haswell Processor (DDR3)



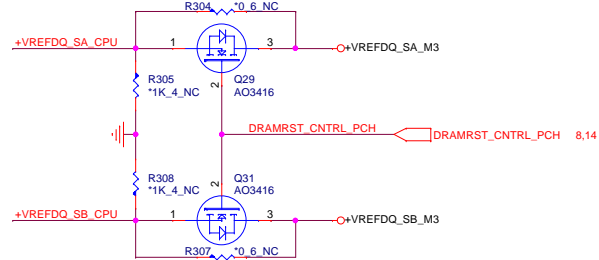
Haswell Processor (DDR3)



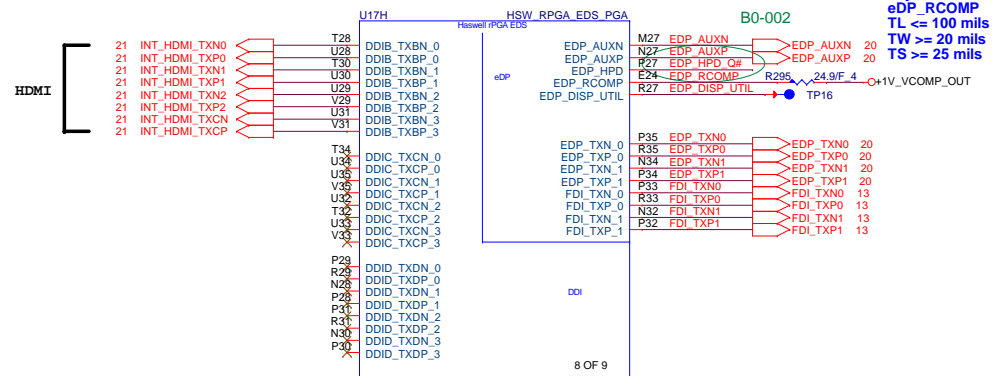
CPU VREFSA M3



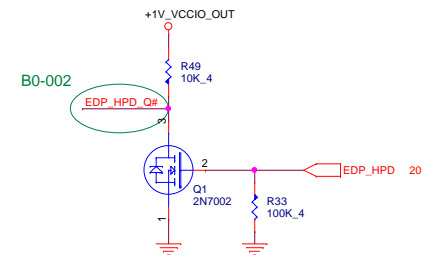
CPU VREFDQ M3



Haswell Processor (DDI,eDP,FDI)



Level Shift



vinafix.com

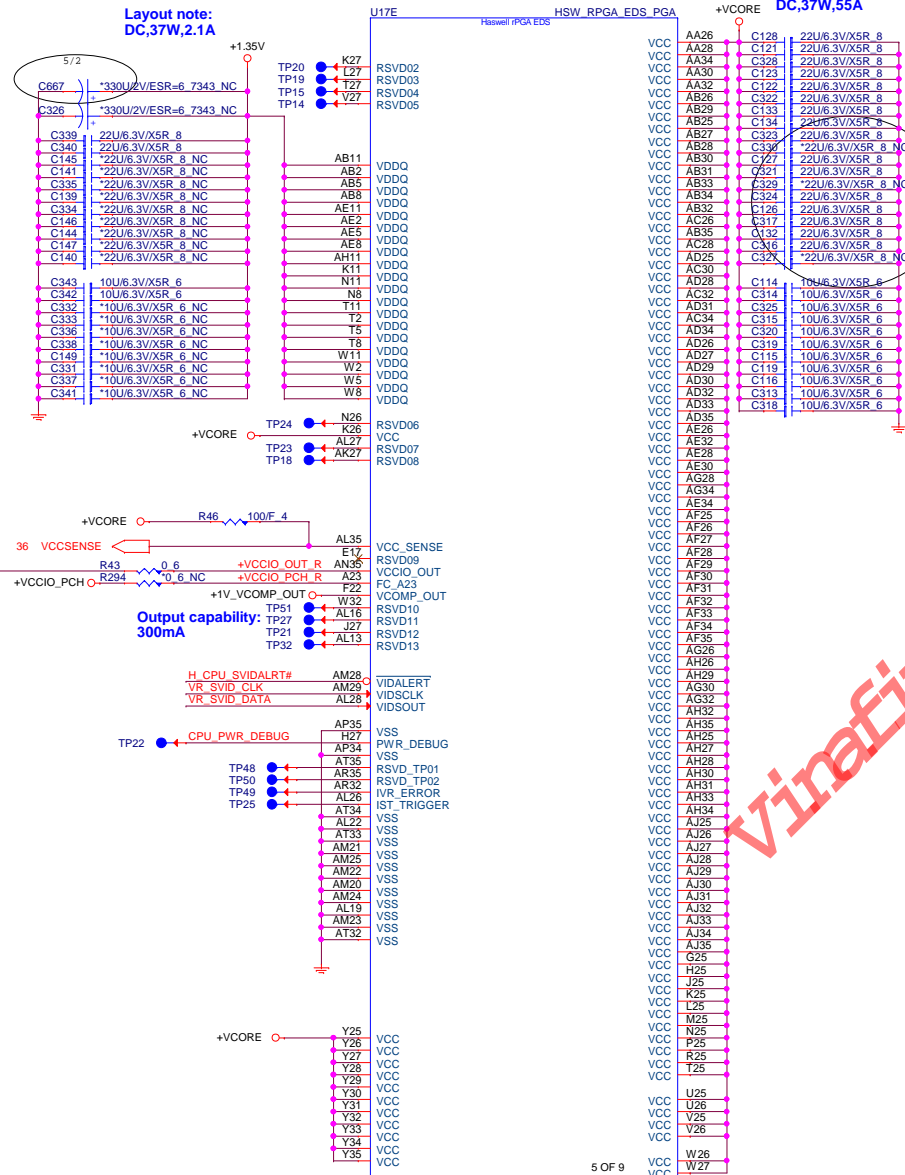


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PROJECT : RR3A

Size	Document Number	Rev
	Haswell 3/5 (DDI/eDP)	D0
Date:	Friday, August 16, 2013	Sheet 10 of 47

Layout note:
DC,37W,2.1A

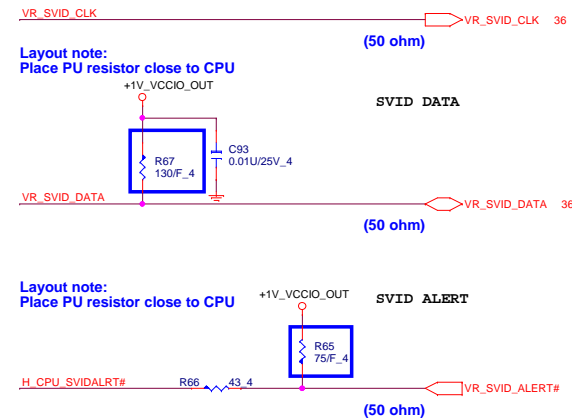


Layout note:
DC,37W,55A

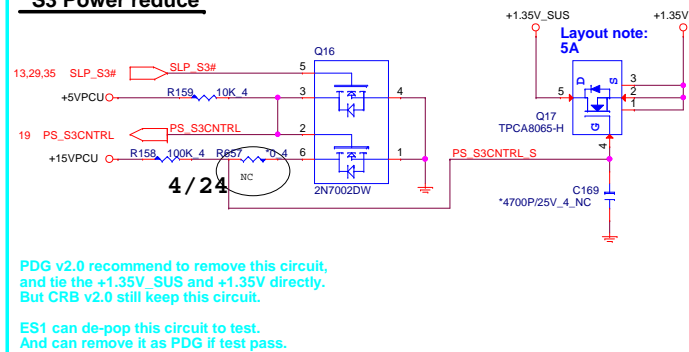
8 / 14

SVID

Layout note:
need routing
together and ALERT need
between CLK and DATA



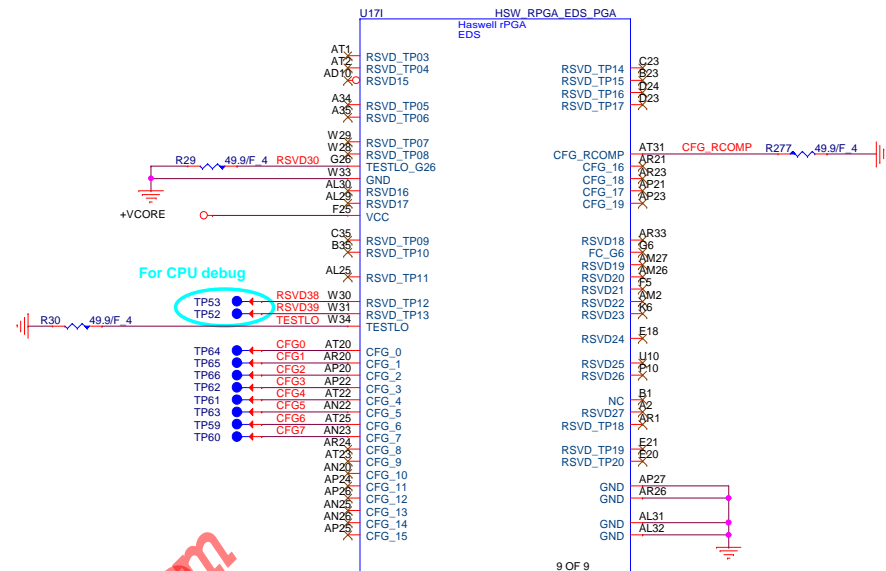
S3 Power reduce



Haswell Processor (GND)



Haswell Processor (CFG,RSVD)



Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	CFG2 R303 *1K 4 NC
CFG[3]	MSR Privacy Bit Feature	x1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting x0 = IA32_Debug_Interface_MSR (0xC80) bit[0]. Default setting overridden	CFG3 R301 *1K 4 NC
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	CFG4 R300 *1K 4
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	CFG6 R296 *1K 4 NC CFG5 R302 *1K 4 NC
CFG[7]			CFG7 R299 *1K 4 NC

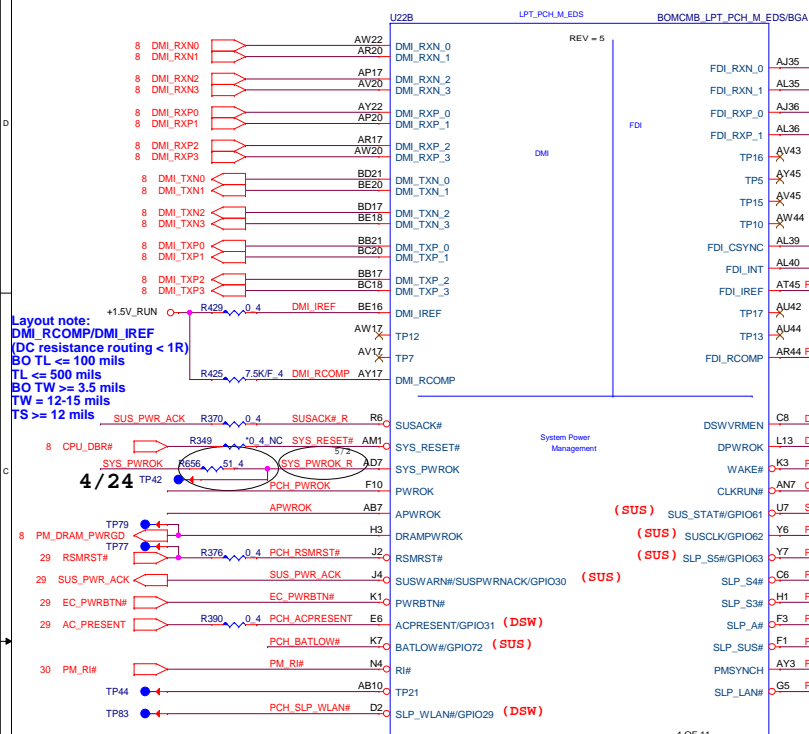


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PROJECT : RR3A

Size	Document Number	Rev
	Haswell 5/5 (CFG/GND)	D0
Date:	Friday, August 16, 2013	Sheet 12 of 47

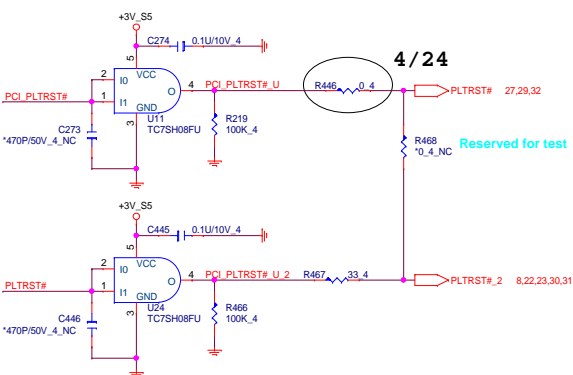
Lynx Point (DMI,FDI,PM)



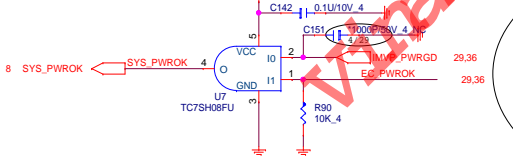
PCH POWOK



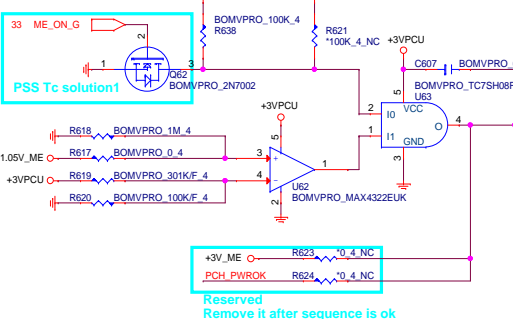
PLTRST# Buffer



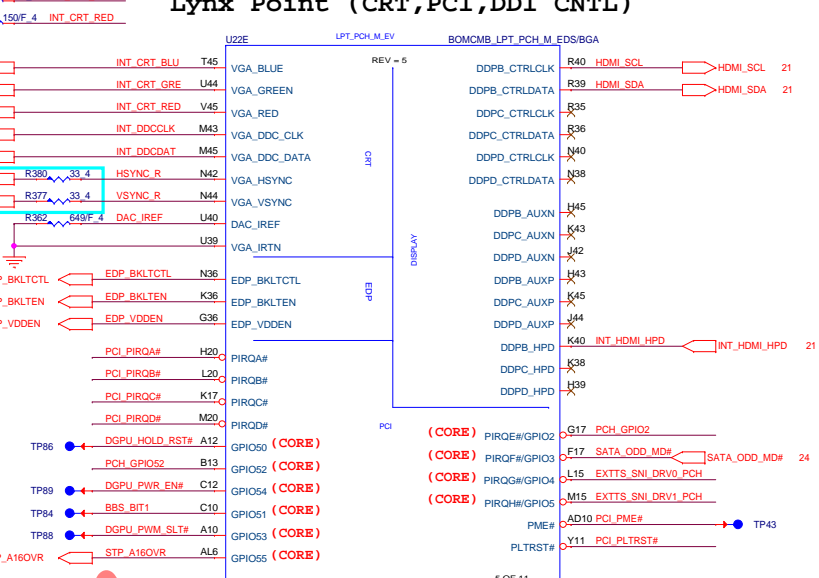
SYSPWOK



APWROK

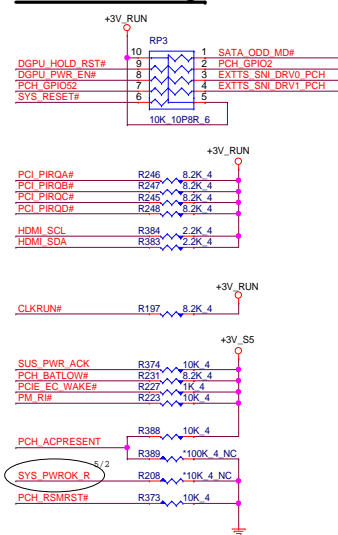


Lynx Point (CRT,PCI,DDI CNTL)

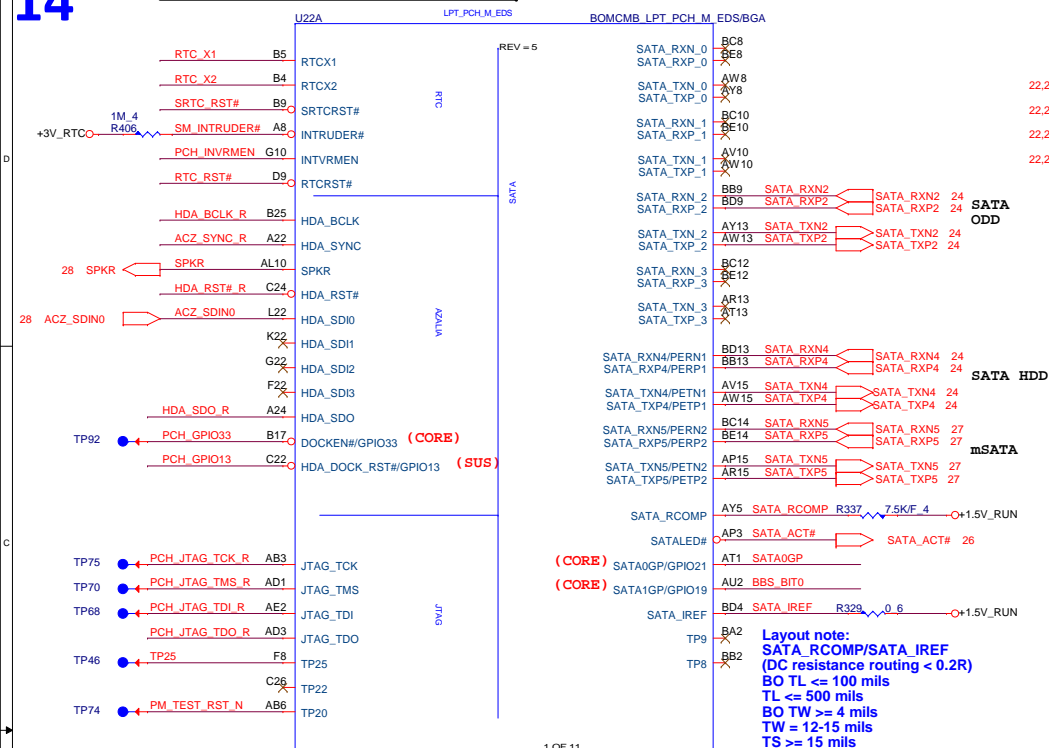


Mode	PCH(U22)
vPRO *	AJ0QE980T00 IC CTRL(695P)QM87 PCH QE98(FCBGA)KEN BSQ
nonvPRO	AJ0QE9A0T05 IC CTRL(695P)HM86 PCH QE9A(FCBGA)KEN BSQ

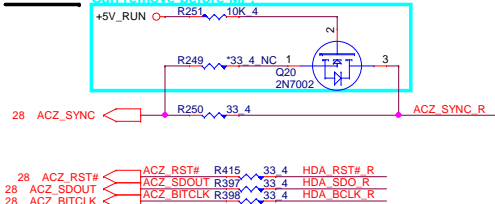
PCH PU/PD setting



Lynx Point (RTC,IHDA,SATA,JTAG)



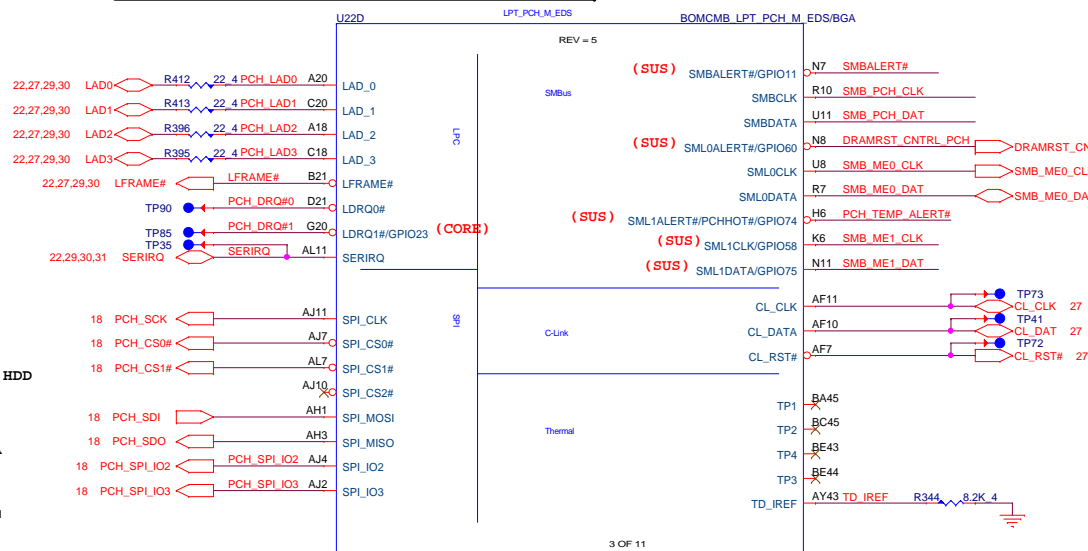
HDA



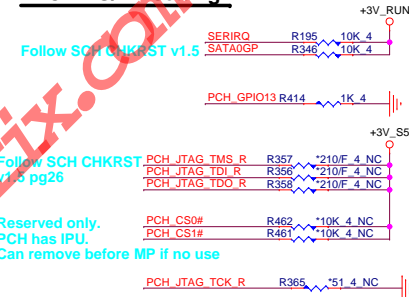
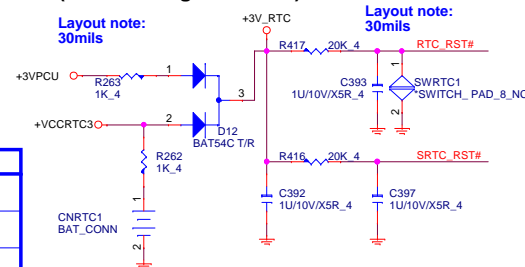
PCH STRAPING

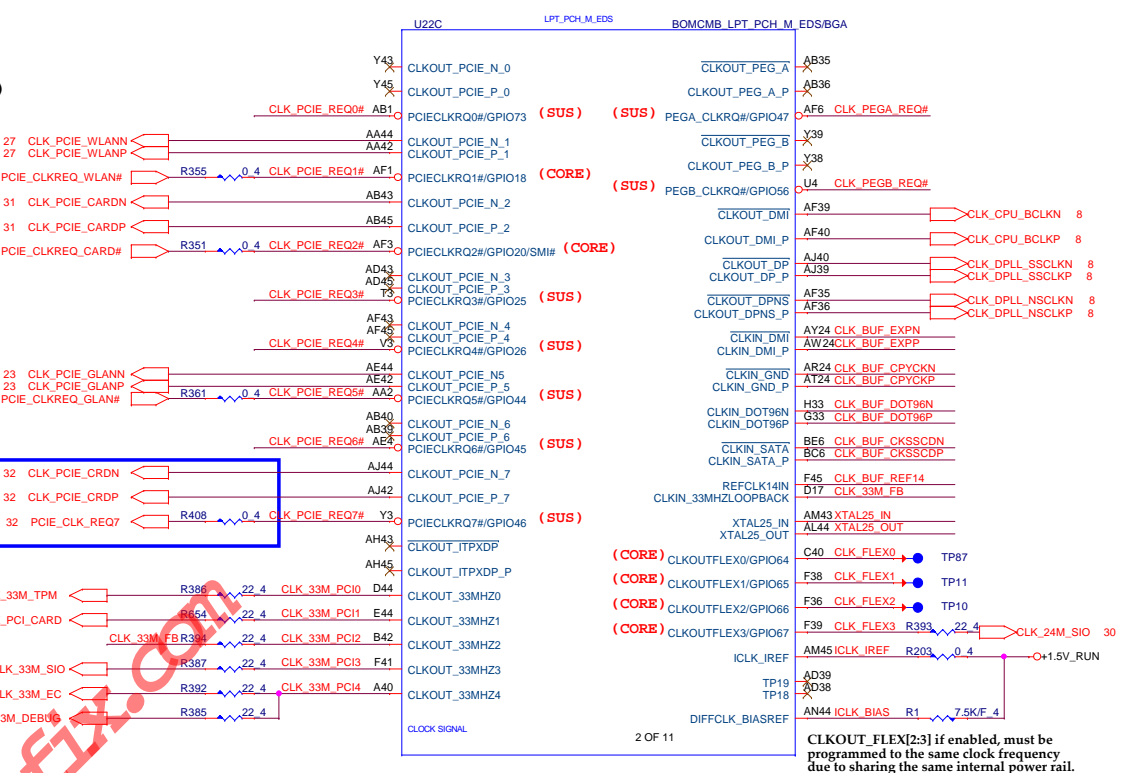
Pin Name	Usage	Sampled	Configuration	Circuitry
SPKR	No Reboot	PWROK	0 = Disable (Int PD) 1 = Enable	SPKR R343 *1K 4 NC +3V_RUN
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	13.22 SUSCLK R210 *1K 4 NC
GPIO55	Top-Block Swap Override	PWROK	0 = Top-Block Swap mode 1 = Default (Int PU)	13 STP_A16OVR R199 *1K 4 NC
INTVRMEN	Integrated VRM Enable	Always	0 = Disable 1 = Enable	PCH_INVRMEN R411 330K 4 +3V_RTC
GPIO51	Boot BIOS Strap bit 1	PWROK	Bit1 Bit0 1 1 Reserved 1 1 SPI 0 0 LPC	BBS_BIT0 R335 10K 4 +3V_RUN
SATA1GP/GPIO19	Boot BIOS Strap bit 0	PWROK		
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	HDA_SDO R405 1K 4 ME_OVERRIDE 29
DSWVREN	On Die DSW VR Enable	Always	0 = Disable 1 = Enable Must be PU to VCCRTC	13 DSWVREN R407 330K 4 R400 330K 4 NC +3V_RTC



Lynx Point (LPC,SPI,SMBUS,C-LINK,THERMAL)






PCH PU/PD setting



RTC Circuitry
(non Rechargeable BATT)







22 CLK_33M_TPM  R386 

31 CLK_PCI_CARD  R554 

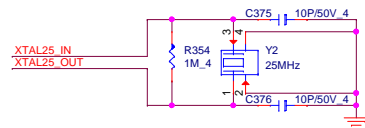
CLK_33M_FB R394 

30 CLK_33M_SIO  R387 

29 CLK_33M_EC  R392 

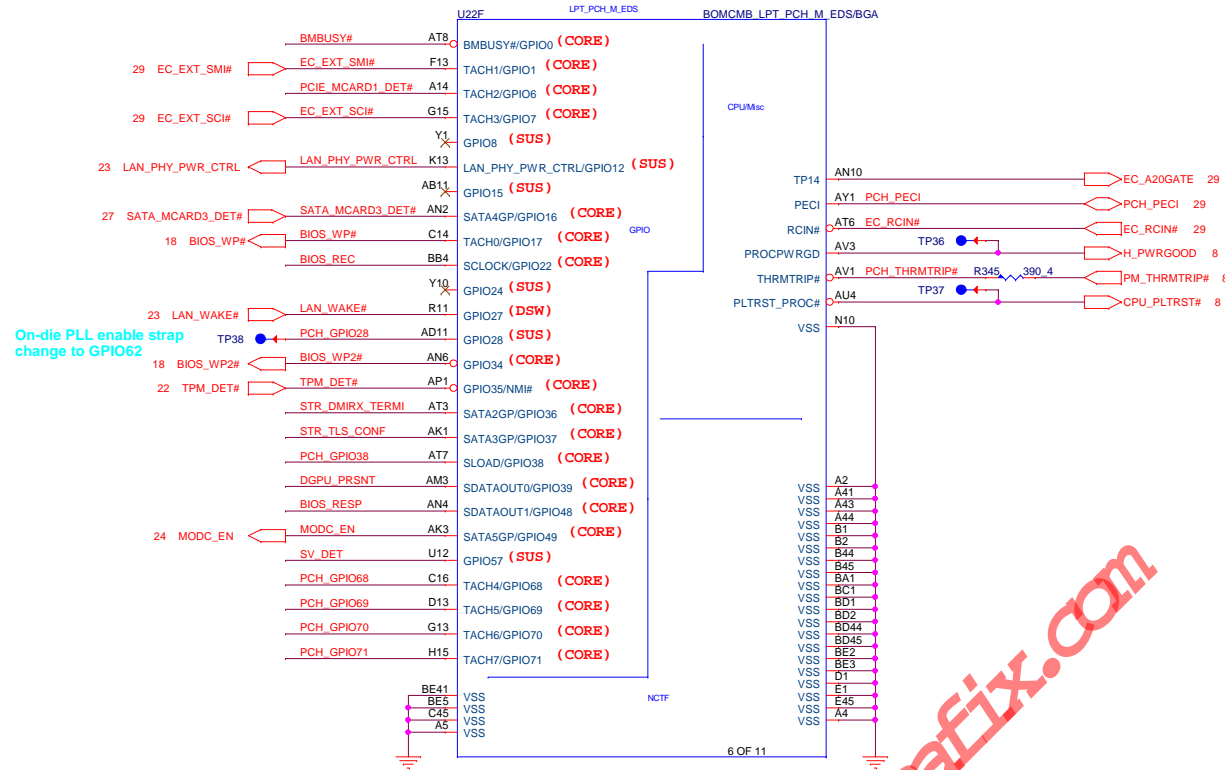
27 CLK_33M_DEBUG  R385 

Pin	Function	Value
CLK_PCIE_REQ0#	R359	10K 4
CLK_PCIE_REQ4#	R216	10K 4
CLK_PCIE_REQ5#	R360	10K 4
CLK_PCIE_REQ6#	R353	10K 4
CLK_PCIE_REQ7#	R215	10K 4
CLK_PEGA_REQ#	R348	10K 4
CLK_PEGB_REQ#	R218	10K 4
USB_OC#	R369	10K 4
USB_OC7#	R371	10K 4
CLK_PCIE_REQ3#	R220	10K 4
CLK_BUF_EXP_N	R187	10K 4
CLK_BUF_EXPP	R188	10K 4
CLK_BUF_CPYCKN	R190	10K 4
CLK_BUF_CPYCKP	R189	10K 4
CLK_BUF_DOT16N	R221	10K 4
CLK_BUF_DOTSDP	R228	10K 4
CLK_BUF_CKSDCPN	R330	10K 4
CLK_BUF_CKSDCP	R331	10K 4
CLK_BUF_REF14	R226	10K 4



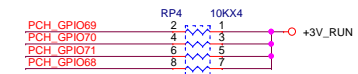
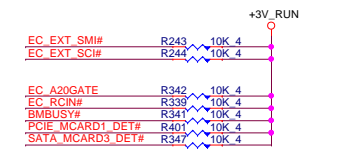
CLK 33M EC	EC61	*10P/50V 4 NC
CLK 33M DEBUG	EC56	*10P/50V 4 NC
CLK 33M FB	EC63	*10P/50V 4 NC
CLK 33M TPM	EC57	*10P/50V 4 NC
CLK 33M SIO	EC58	22P/50V 4
CLK 24M SIO	EC62	22P/50V 4

Lynx Point (GPIO,CPU/MISC,NCTF)



PCH PU/PD setting

TPM_DET# R3 10K 4 +3V_RUN
wTPM: Drive to L by tied to GND on DB side.
woTPM: Drive to H by PU.(pin open)



PCH Strap

Pin Name	Usage	Sampled	Configuration	Ref. Doc.	Circuitry
SATA2GP / GPIO36	DMI RX Termination	Rising edge of PWROK	0 = DMI RX is terminated to VSS. 1 = DMI RX is terminated to VCC2.	PCH EDS v1.5 SCH CHKLST v1.5	STR_DMIRX_TERMI R196 10K 4 R194 200K 4 NC +3V_RUN
SATA3GP / GPIO37	TLS Confidentiality	Rising edge of PWROK	0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).	PCH EDS v1.5 SCH CHKLST v1.5	STR_TLS_CONF R334 BOMNONV 100K 4 R328 BOMVPRO 1K 4 +3V_RUN nonvPRO(Non-iAMT): PD vPRO(iAMT): PU B0-001

BIOS RECOVERY



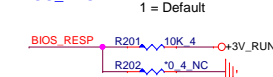
SV Detect



External Gfx Present



BIOS_RESP

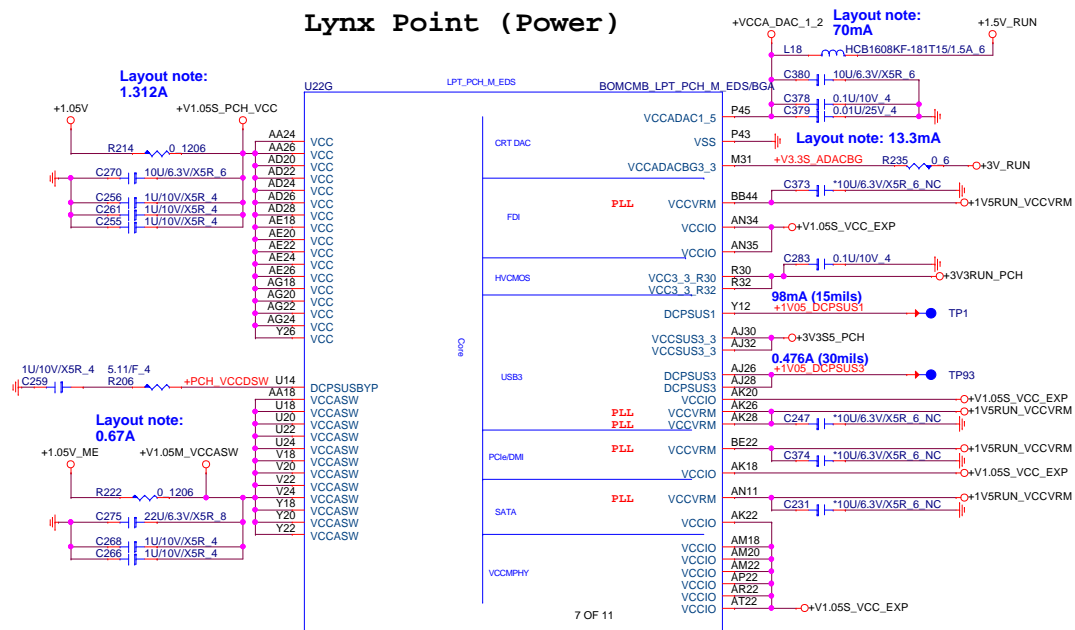


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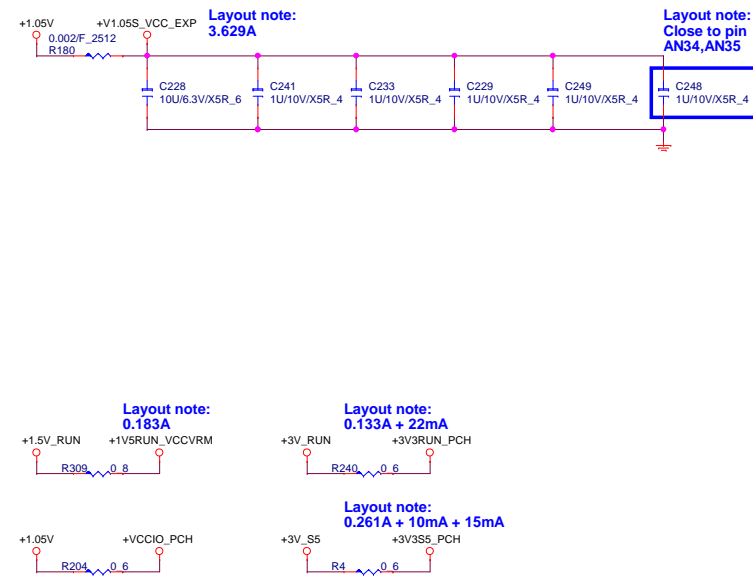
PROJECT : RR3A

Size	Document Number	Rev
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Date:	Friday, August 16, 2013	Sheet 16 of 47

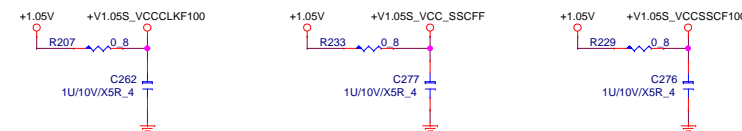
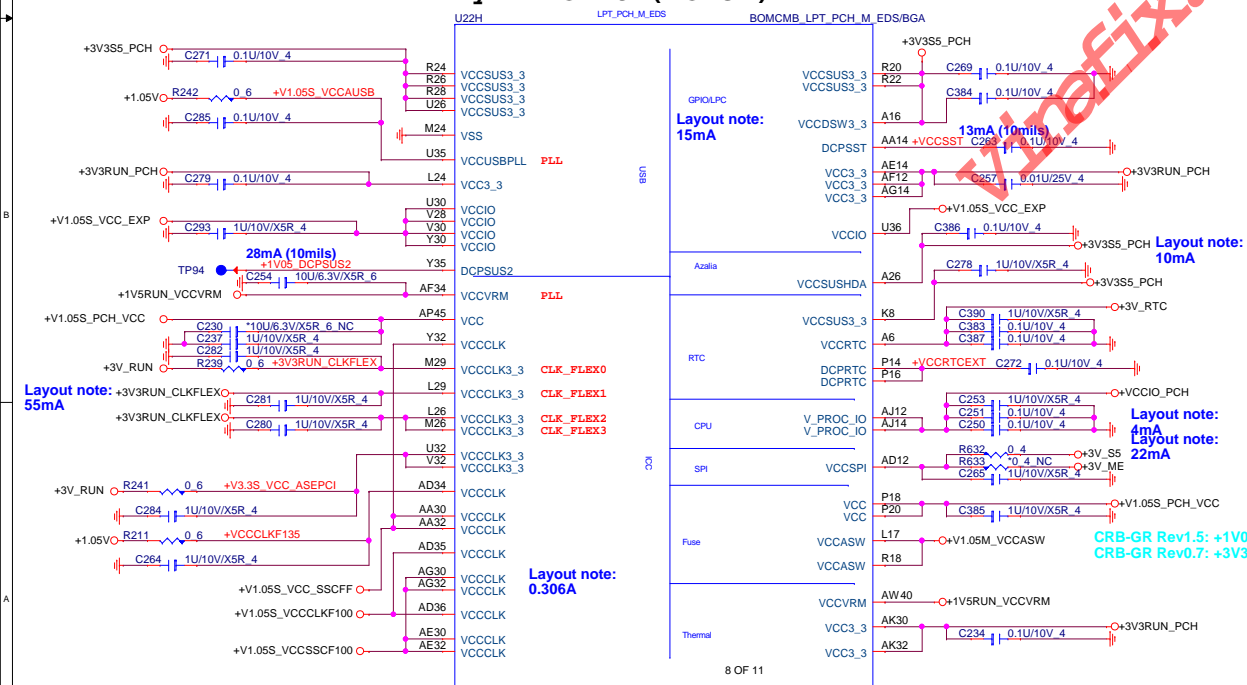
Lynx Point (Power)



PCH VCCIO Power

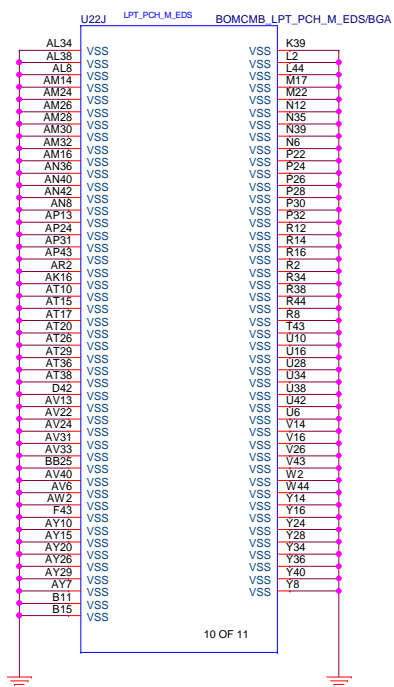


Lynx Point (Power)

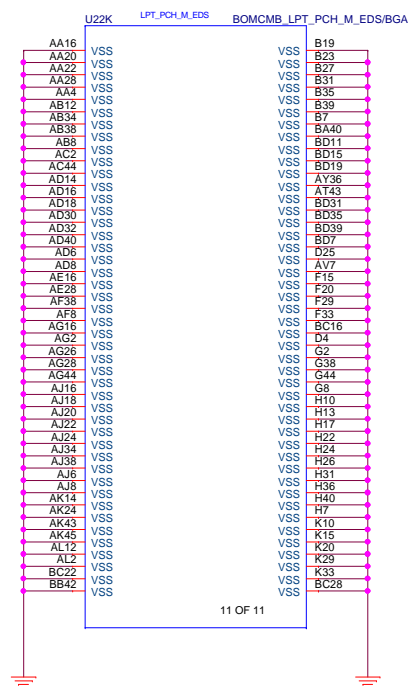


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PROJECT : RR3A

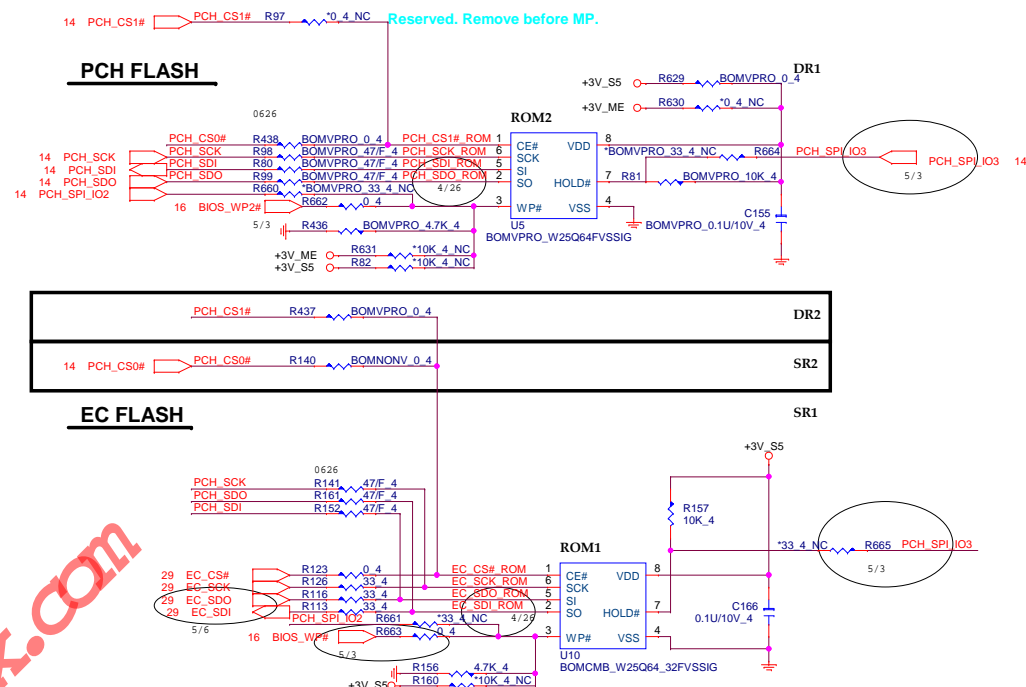
Lynx Point (GND)



Lynx Point (GND)



BIOS/ME/EC FLASH



Mode	SR1	SR2	DR1	DR2	ROM1 QPN	ROM2 QPN
vPRO Dual ROM *	Pop	NC	Pop (Except R82, R630 and R631)	Pop	AKE391P0N01 IC FLASH(8P)W25Q32FVSSIG(SOIC) 4MB, BIOS+EC (PCH CS1#)	AKE3EFP0N06 8MB, ME(5MB) (PCH CS0#)
nonvPRO Share ROM	Pop	Pop	NC	NC	AKE3EFP0N06 IC FLASH(8P)W25Q64FVSSIG(SOIC) 8MB, BIOS+ME(2MB)+EC (PCH CS0#)	Don't care (NC)

TP for ICT flash BIOS process



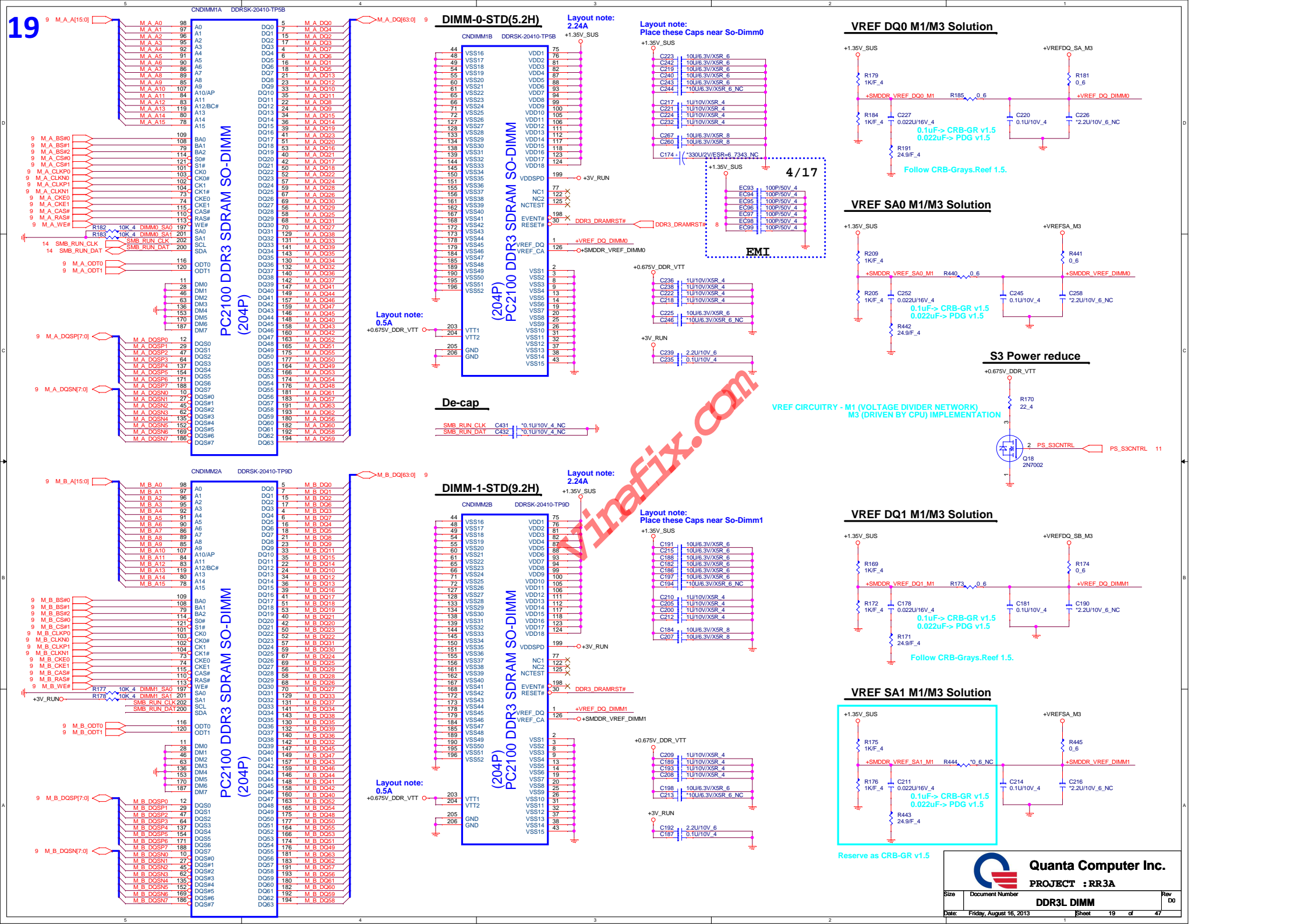
EMI



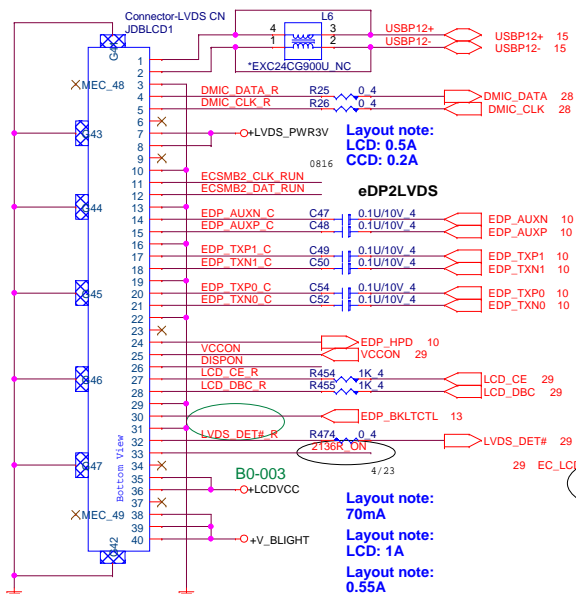
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PROJECT : RR3A

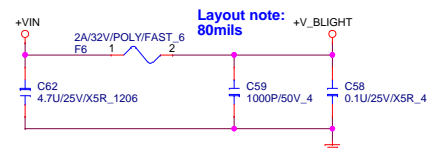
Size	Document Number	Rev
	LPT 6/6 (GND)	D0
Date:	Friday, August 16, 2013	Sheet 18 of 47



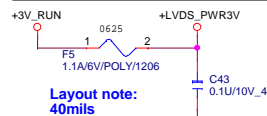
eDP2LVDS DB connector



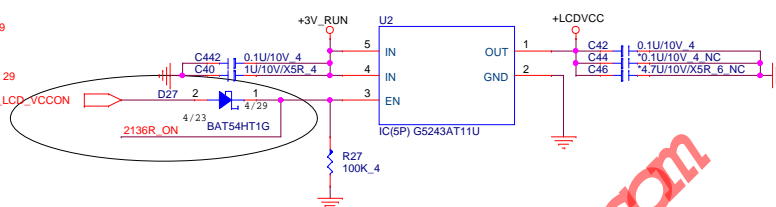
LCD Panel Backlight Power



eDP2LVDS IC, LCD Panel EDID and CCD Power



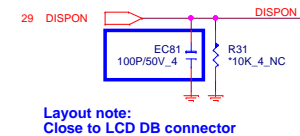
LCD Panel Controller Power



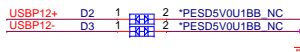
eDP2LVDS IC Power

4/23

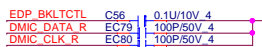
Backlight Enable



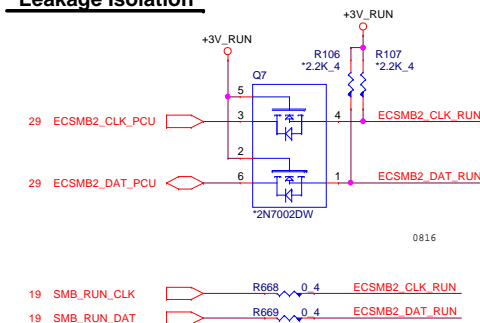
ESD



De-cap

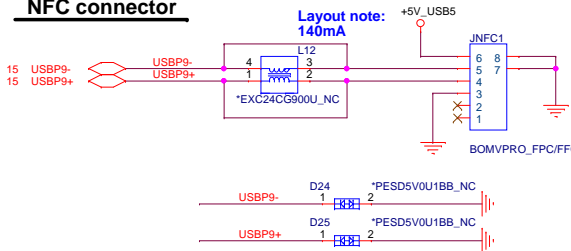


Leakage Isolation

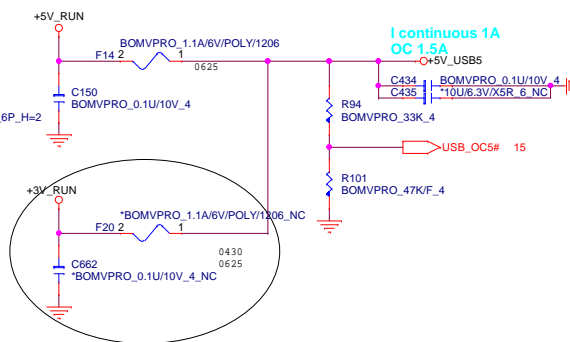


NFC

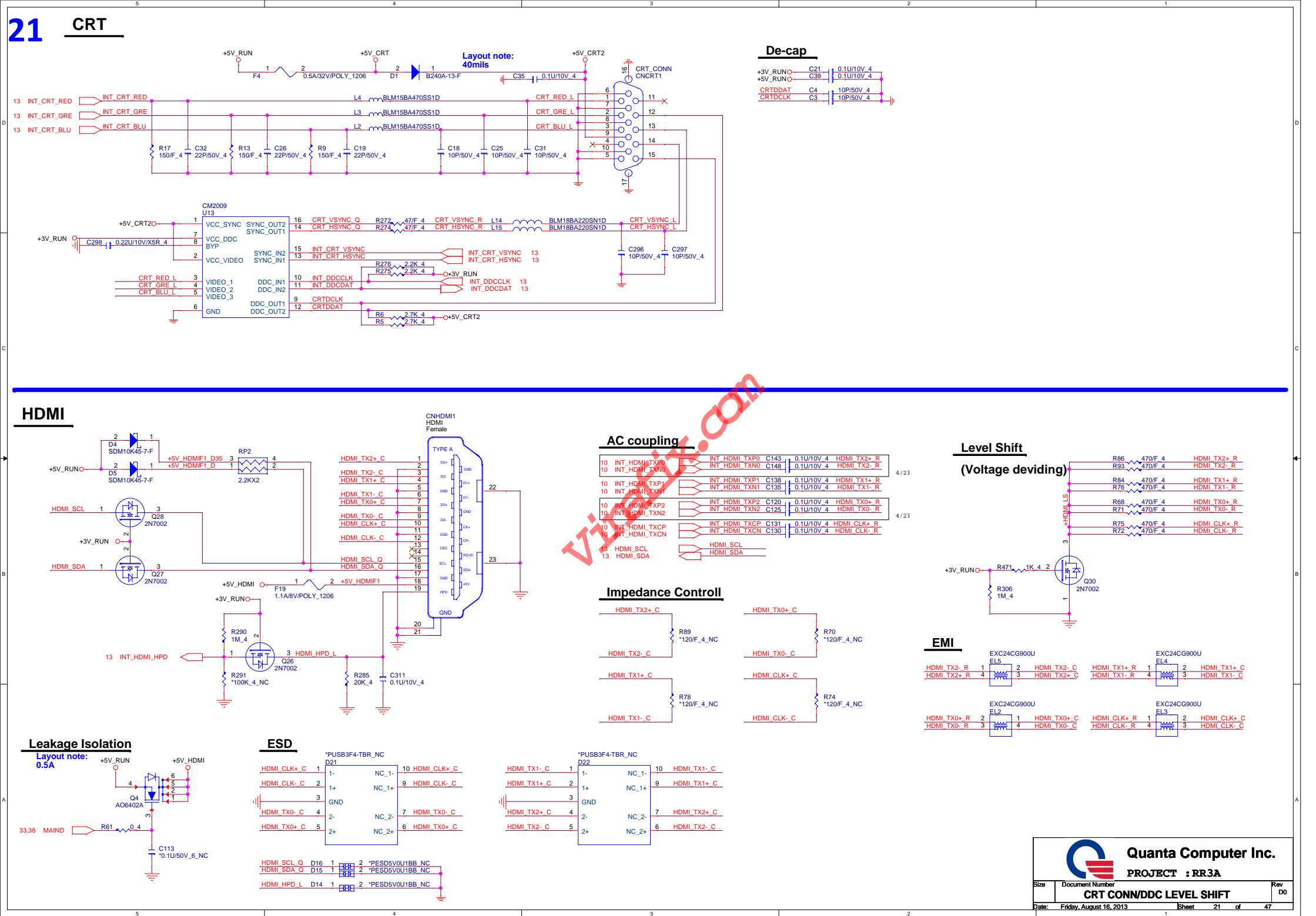
NFC connector

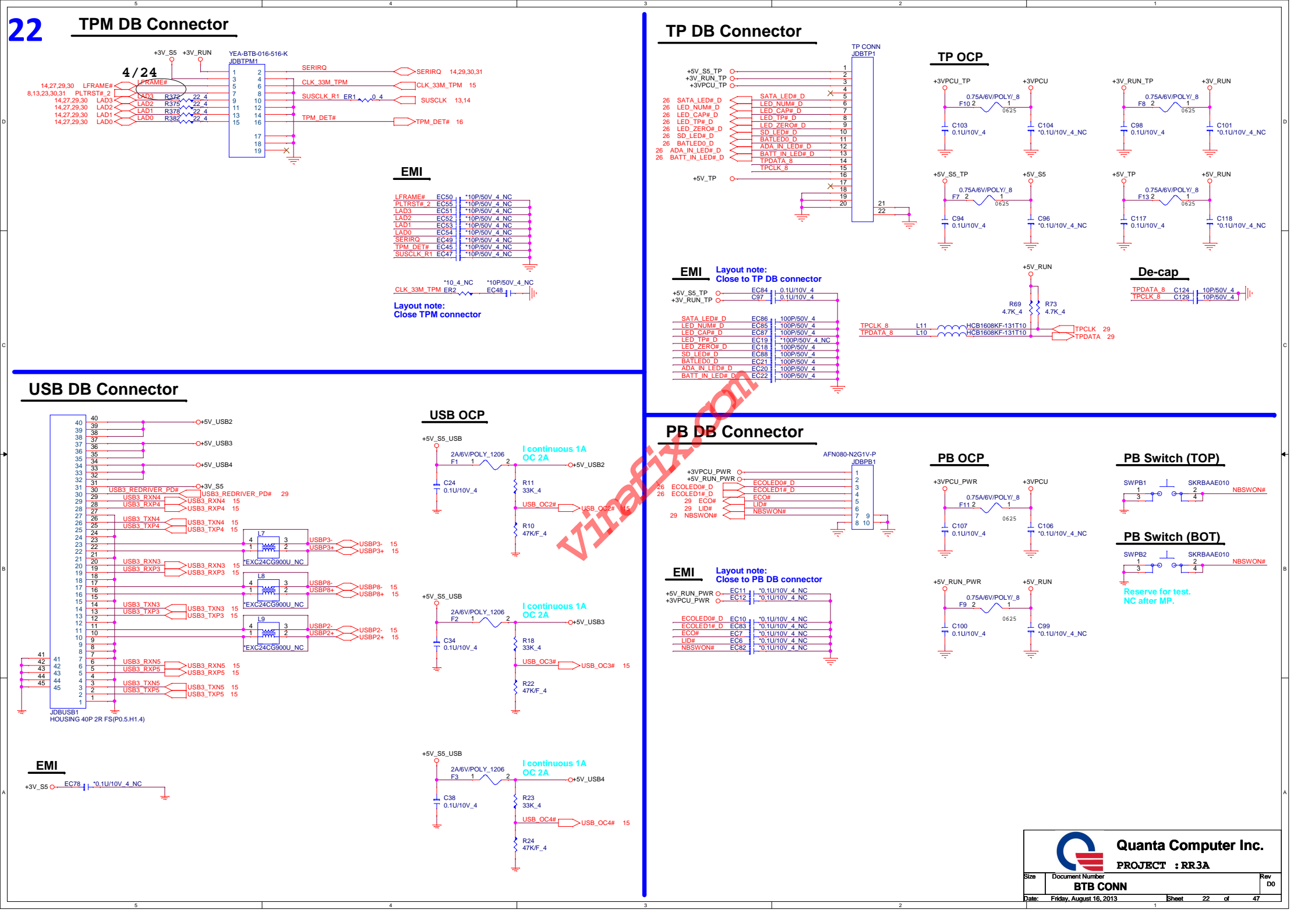


NFC OCP

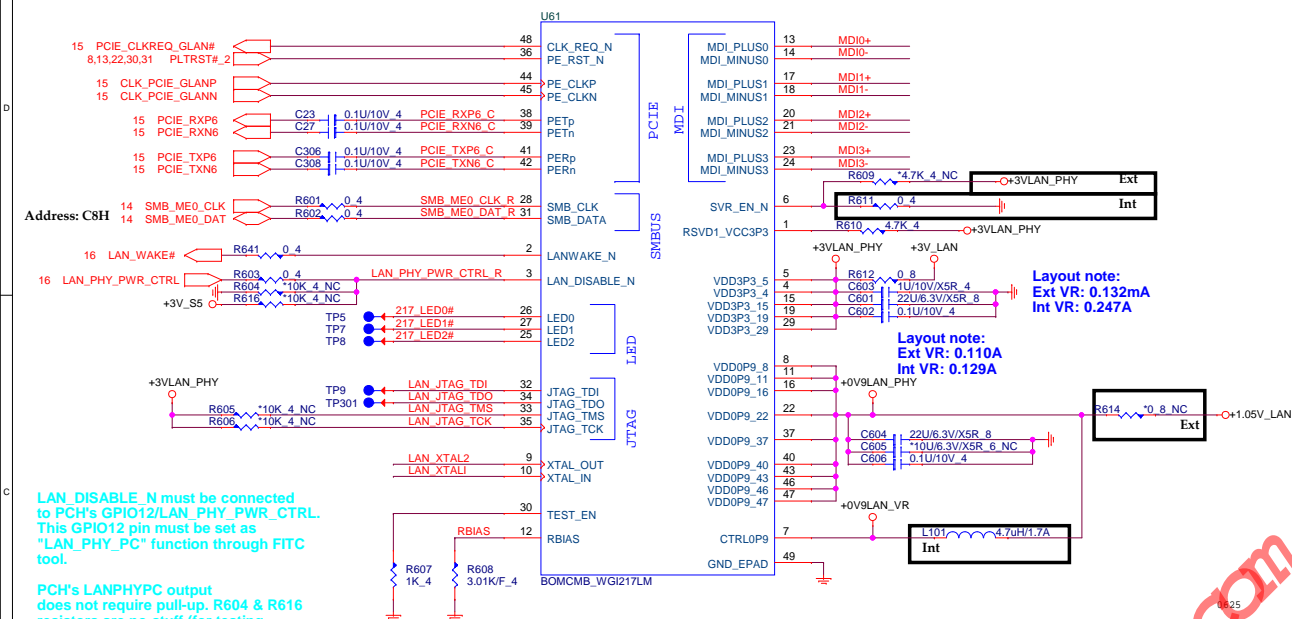


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Controller



LAN_DISABLE_N must be connected to PCH's GPIO12/LAN_PHY_PWR_CTRL. This GPIO12 pin must be set as "LAN_PHY_PC" function through FITC tool.

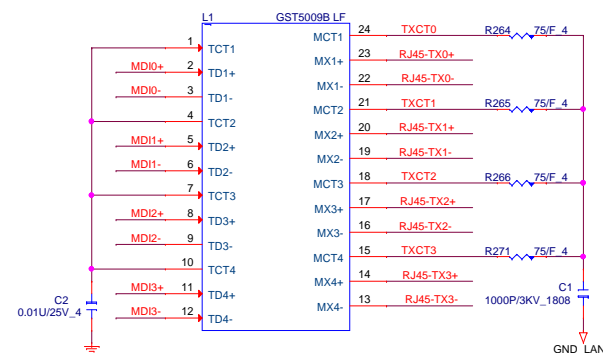
PCH's LANPHYPC output does not require pull-up. R604 & R616 resistors are no-stuff (for testing purpose only).

Mode	LAN(U61)
vPRO *	AL0SLJWE001 IC CTRL(48P)WGI217LM A3 SLJWE(QFN)
nonvPRO	AL0SLJWG001 IC CTRL(48P)WGI217V A3 SLJWG(QFN)

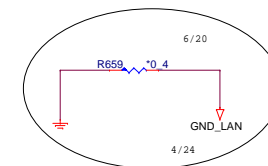
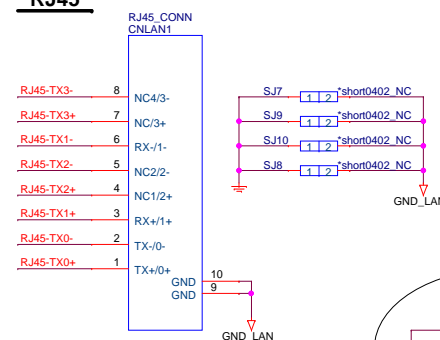
Vpro	Non-Vpro	Mode	R609	R611	R614	L101
*	*	VDD0P9 Int VR	NC	Pop	NC	Pop
		VDD0P9 Ext VR	Pop	NC	Pop	NC

Location

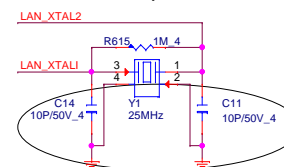
10/100/1000 Transformer



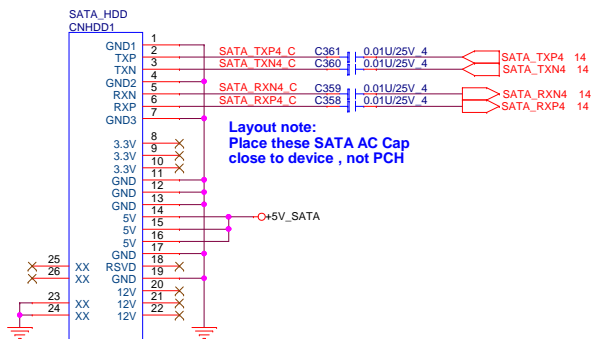
RJ45



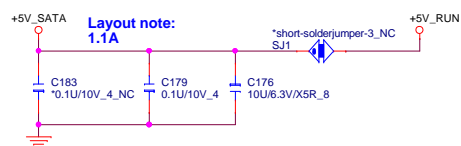
X'tal 25MHz



2.5" SATA HDD

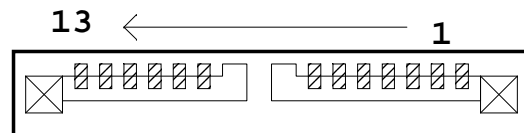
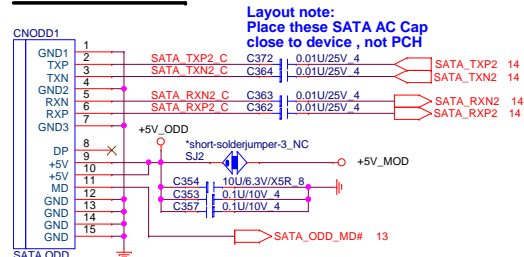


HDD Power

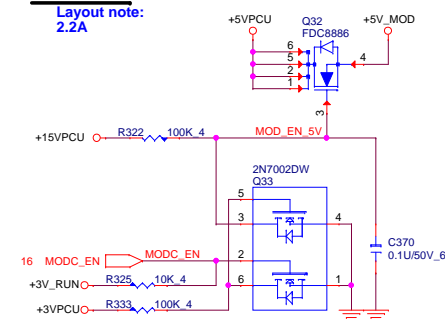


SATA ODD

ODD connector



ZPODD

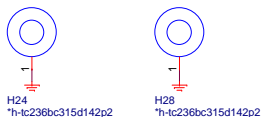
Layout note:
2.2A

Screw

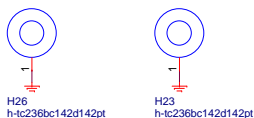
Nut (BOT)

PTH with Ring

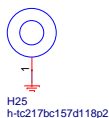
PCH NUT



mSATA NUT

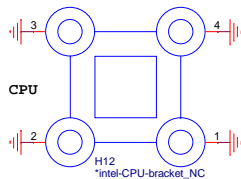


TPM NUT

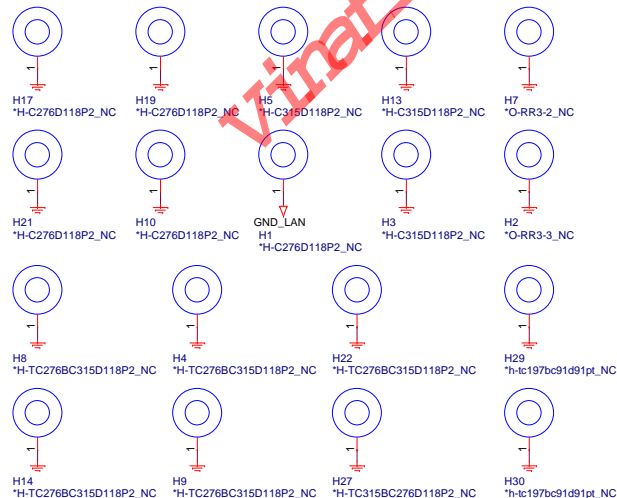


Bracket (TOP)

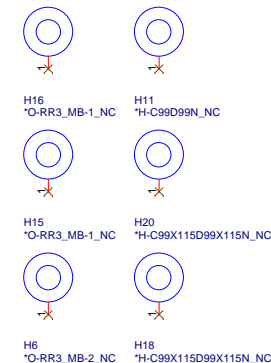
PTH with Ring



PTH with Ring



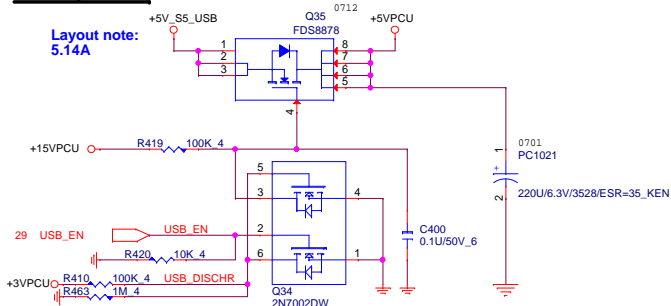
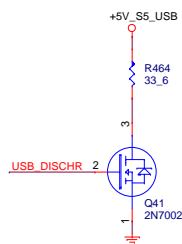
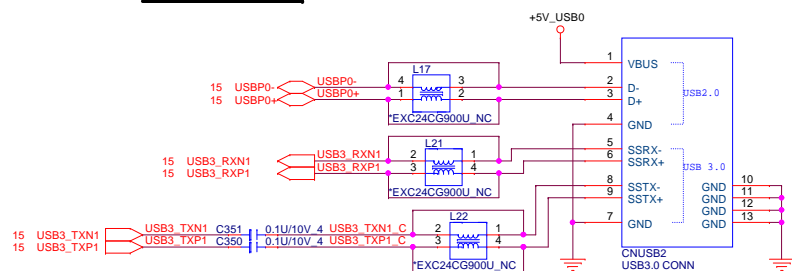
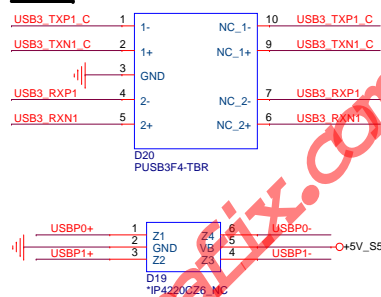
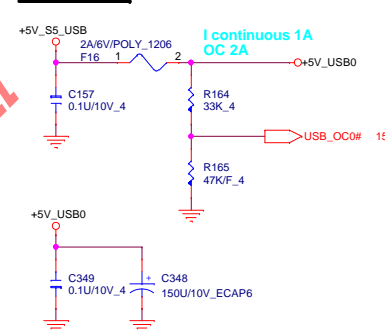
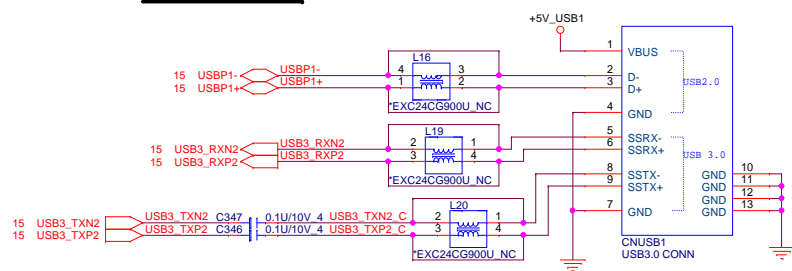
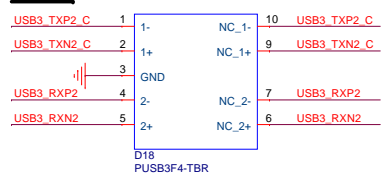
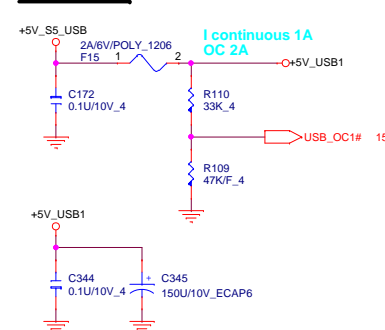
Non-PTH without Ring



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PROJECT : RR3A

Size	Document Number	Rev
	HDD/ ODD/HOLE	D0
Date:	Friday, August 16, 2013	Sheet 24 of 47

USB powerLayout note:
5.14A**Discharging circuit****U3 Connector****ESD****USB OCP****U3 Connector****ESD****USB OCP**

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PROJECT : RR3A

Size Document Number

USB port

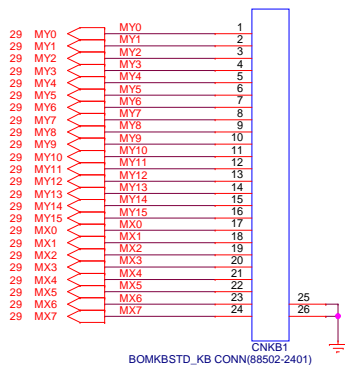
Rev D0

Date: Friday, August 16, 2013

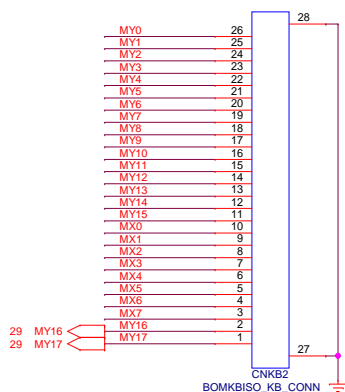
Sheet 25 of 47

Keyboard

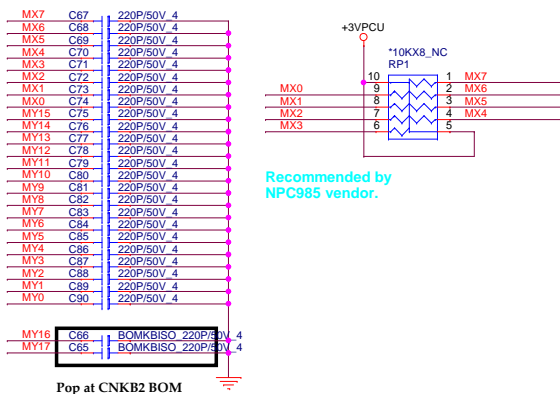
For Standard 87key



For Isolation w/ 10key

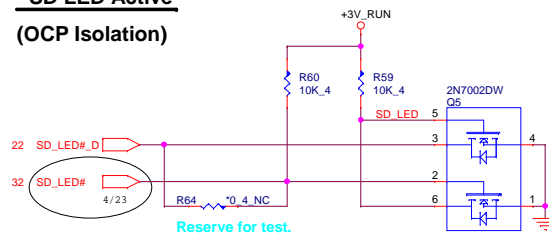


EMI

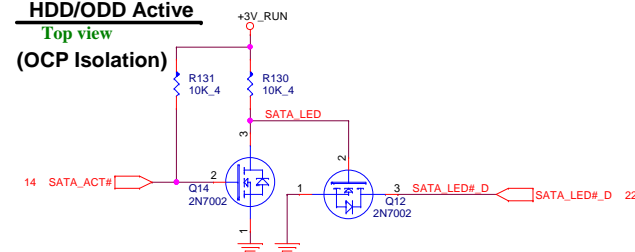


LED of TP DB

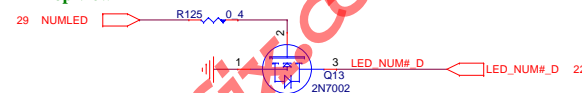
SD LED Active (OCP Isolation)



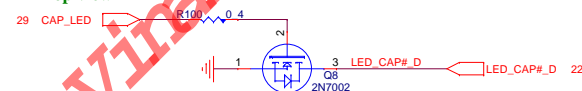
HDD/ODD Active Top view (OCP Isolation)



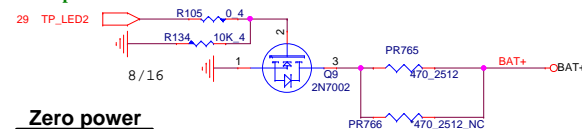
NUM LOCK Top view



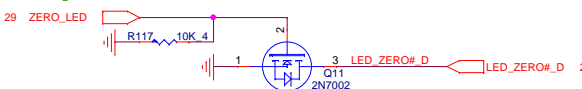
CAP LOCK Top view



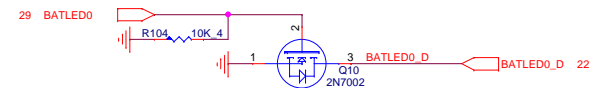
Dummy load for 3cell battery 100% Charge Top view



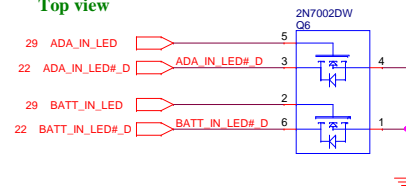
Zero power Top view



Battery Status Top view

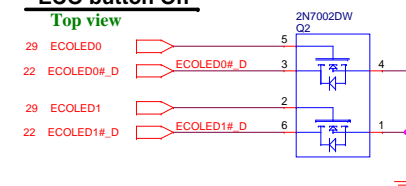


Power Status Top view



LED of TP DB

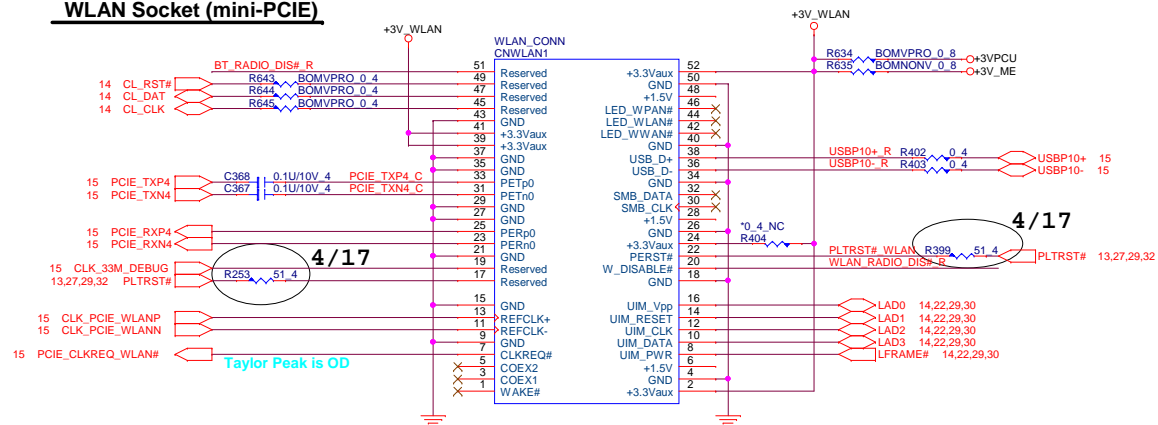
ECO button On Top view



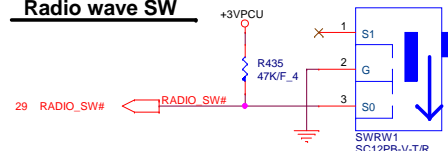
Quanta Computer Inc.

PROJECT : RR3A

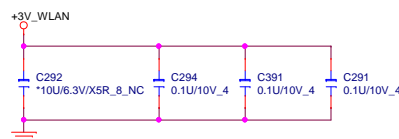
Size	Document Number	Rev
	KB/TP/LED	B0
Date:	Friday, August 16, 2013	Sheet 26 of 44

WLAN Socket (mini-PCIE)

Radio wave SW

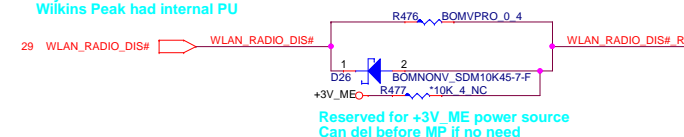


WLAN Power

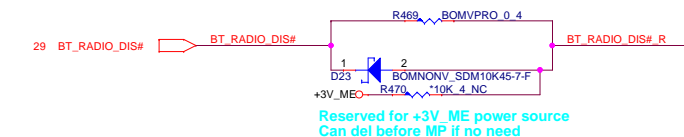


Leakage Isolation

Taylor Peak had internal PU
Wilkins Peak had internal PU

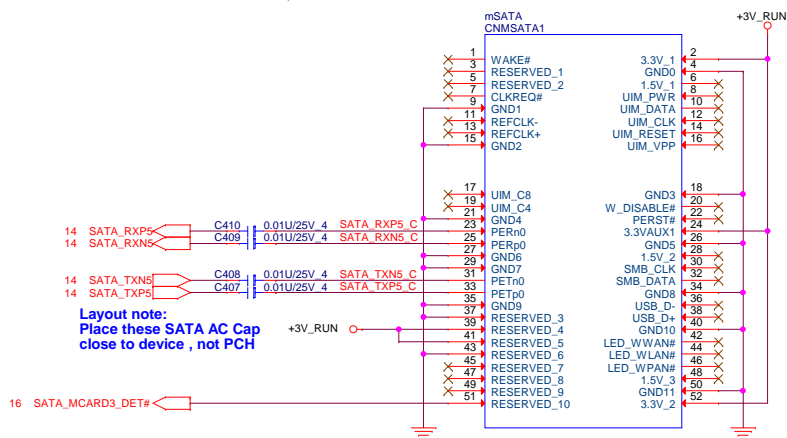


Wilkins Peak had internal PU

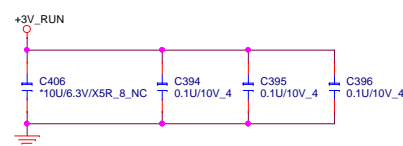


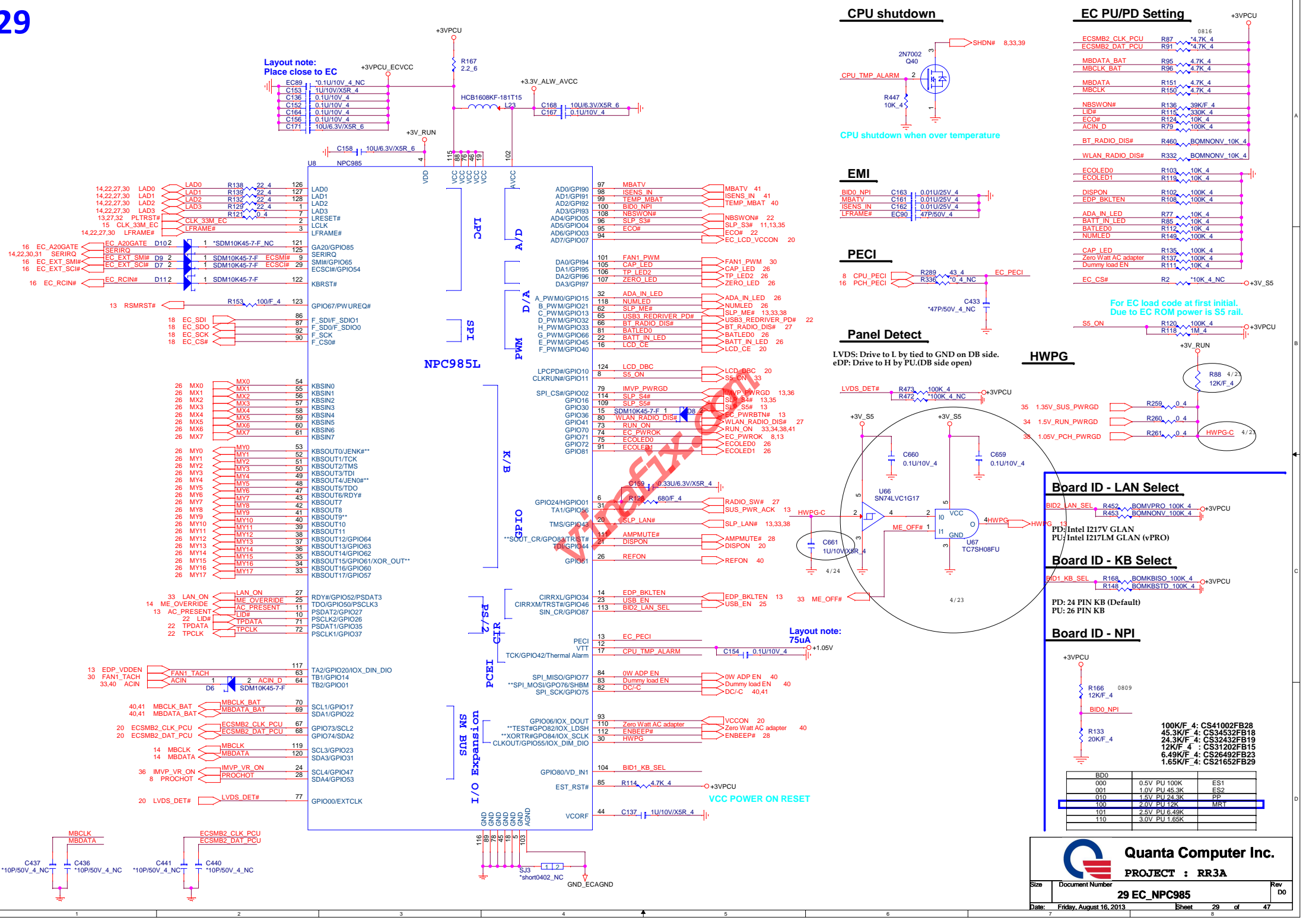
mSATA

mSATA Socket (mini-PCIE)



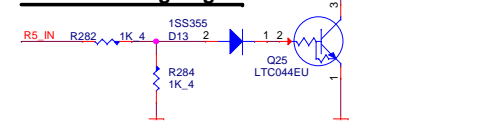
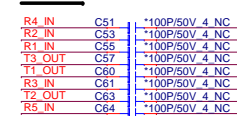
mSATA Power



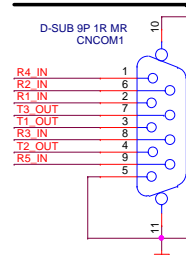




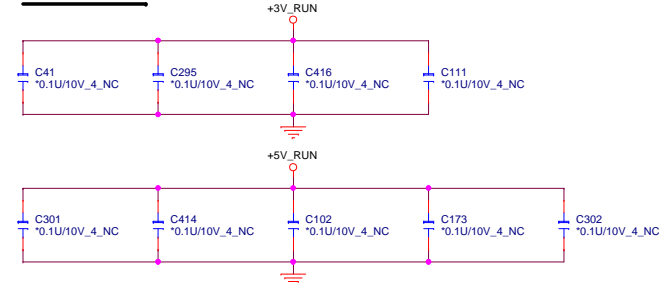
Serial Port

**EMI**

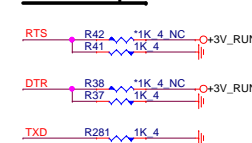
COM Connector



Super IO

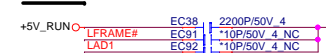


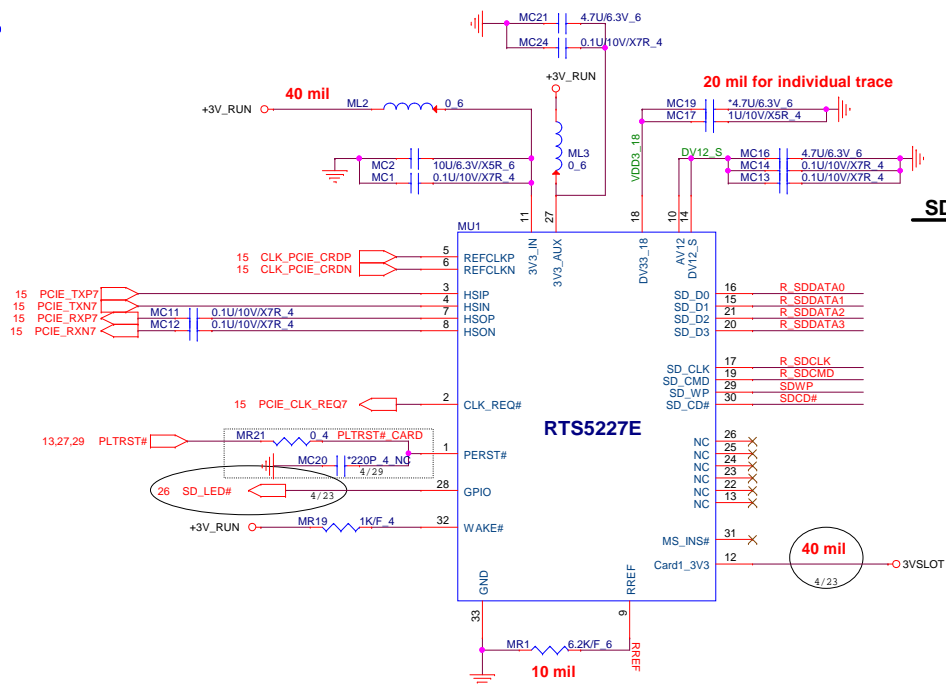
SIO Strap



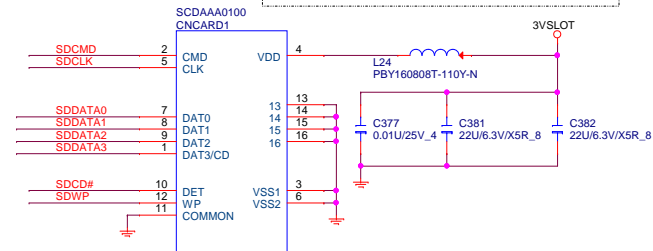
PIN	Name	0	1
15	RTS	2E	4E
16	DTR	24MHz	48MHz
18	TXD	DISABLE	ENABLE

EMI

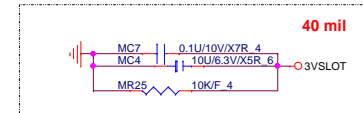




SD Connector

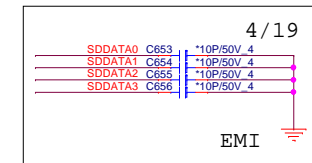
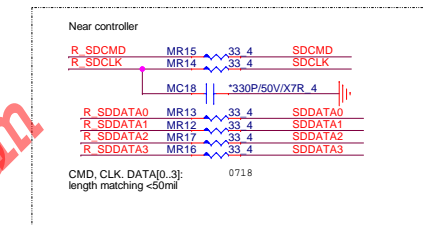


These component need
to close to Slot



MFIO Pin Assignment Table

MFIO	SD8	XD	MS8
00	WP	D7	BS
01	D1	D6	-
02	D0	D5	D1
03	D7	D4	-
04	D6	D3	D5
05	CLK	D2	D0
06	-	D1	-
07	D5	D0	D4
08	CMD	WP#	D2
09	D4	WE#	D6
10	D3	ALE	D3
11	D2	CLE	-
12	-	CE#	-
13	-	RE#	D7
14	-	R/B#	CLK



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PROJECT : RR3A

Size	Document Number	Rev
	CARD_527E	D0

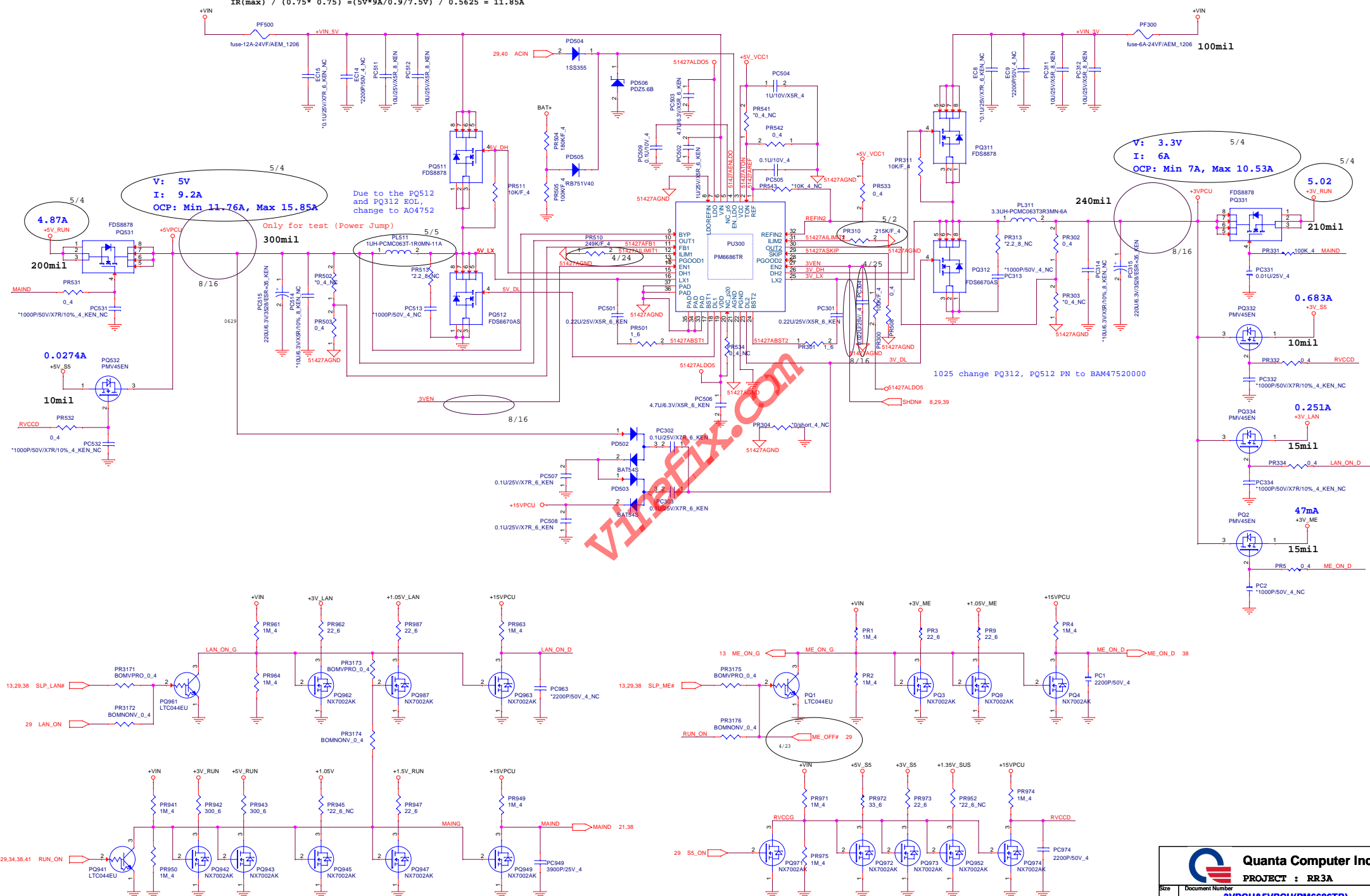
Date: Friday, August 16, 2013 Sheet 32 of 47

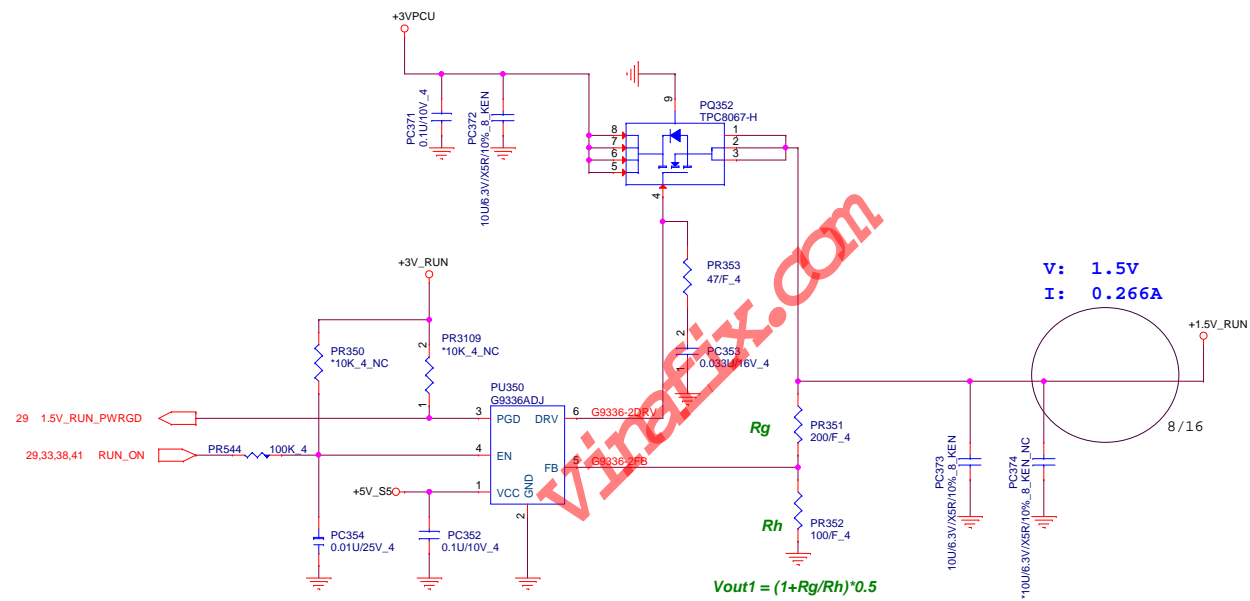
33 3.3V & 5V

$$\text{Fuse Rating} = \text{IR(max)} / (0.75 * 0.75) = (5\text{V} * 9\text{A} / 0.9 / 7.5\text{V}) / 0.5625 = 11.85\text{A}$$

Fuse Rating =

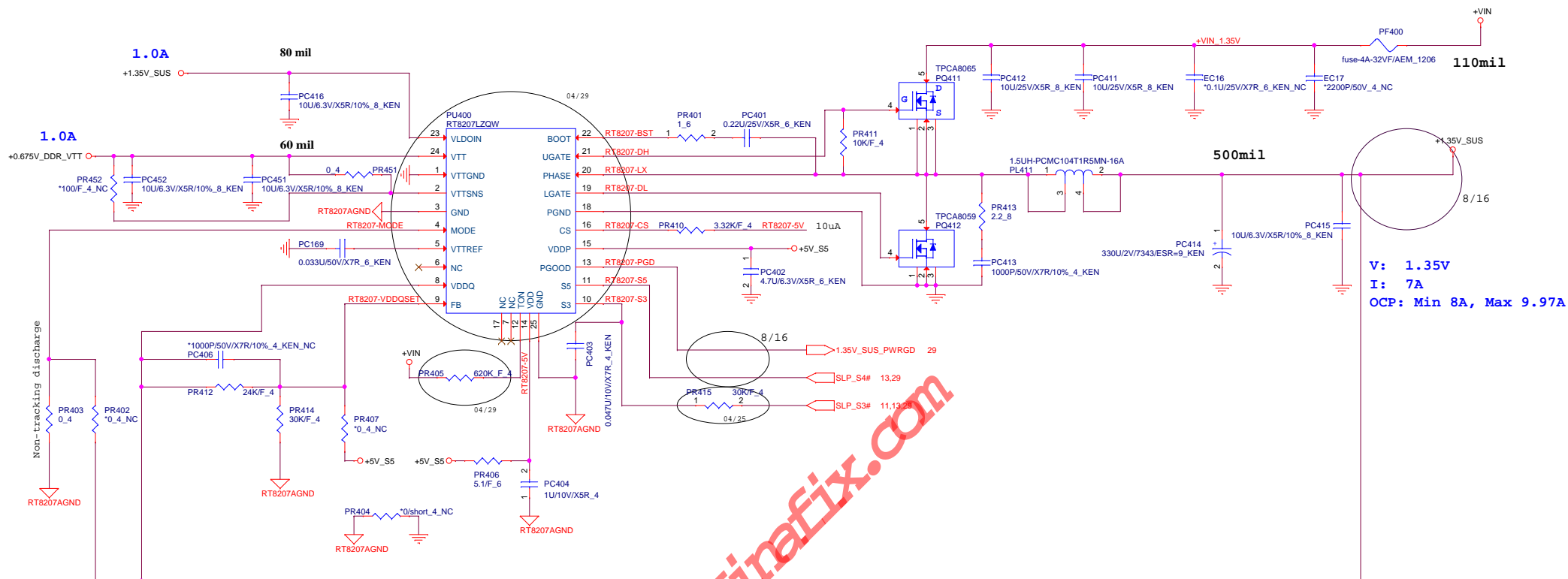
$$IR(max) / (0.75 * 0.75) = (3.3V * 4.8A / 0.9 / 7.5V) / 0.5625 = 4.17A$$





1.35VSUS & VTT_MEM

$$\text{Fuse Rating} = \frac{\text{IR(max)}}{(0.75 * 0.75)} = \frac{(1.35V * 7A / 0.9 / 7.5V)}{0.5625} = 2.48A$$



V: 1.35V
I: 7A
OCP: Min 8A, Max 9.97A

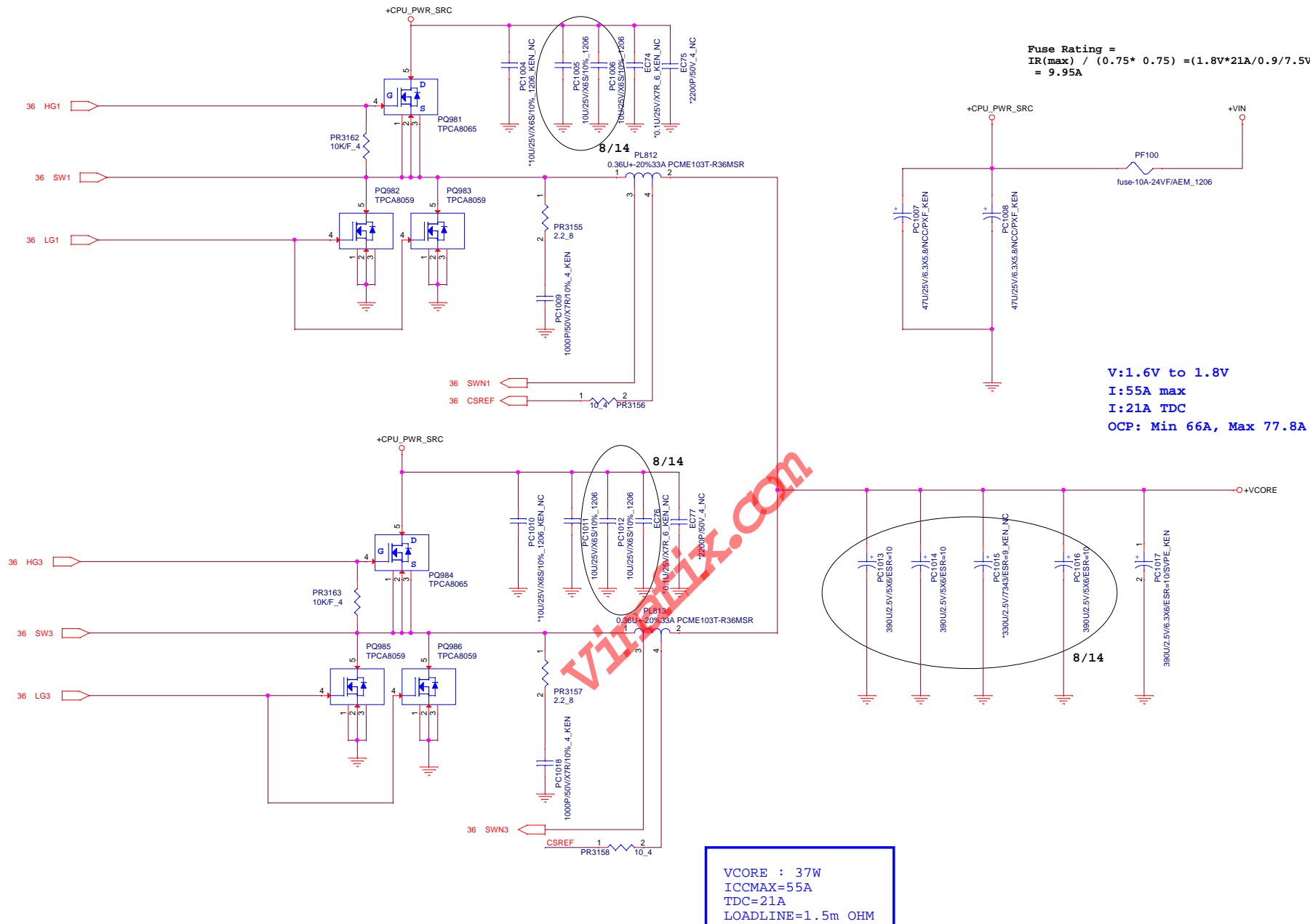
MODE	DISCHARGE MODE
+5V	No discharge
+1.35V	Tracking discharge
GND	Non-tracking discharge

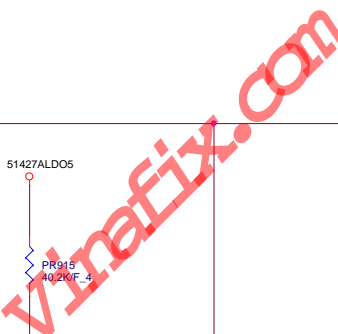
VDDQSET	VDDQ(V)	VTTREF & VTT	NOTE
GND	1.5 fixed	VDDQSNS/2	DDR3
5V	1.8 fixed	VDDQSNS/2	DDR2
FB-Resistor	Adjustable	VDDQSNS/2	1.2V < VDDQ < 3V

$$VTT = VTTREF = VDDQSNS/2 = 0.675V$$

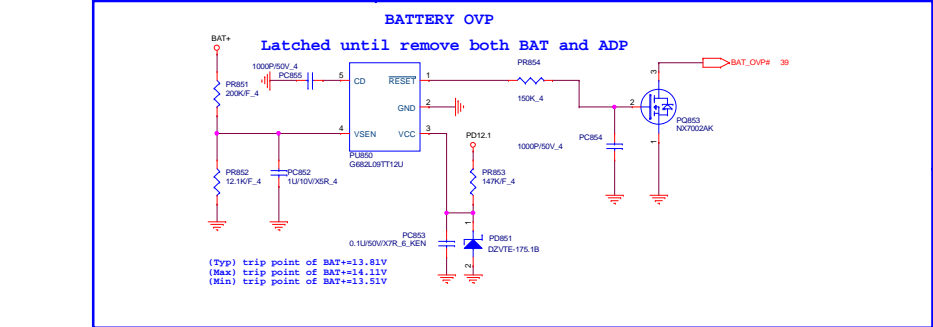
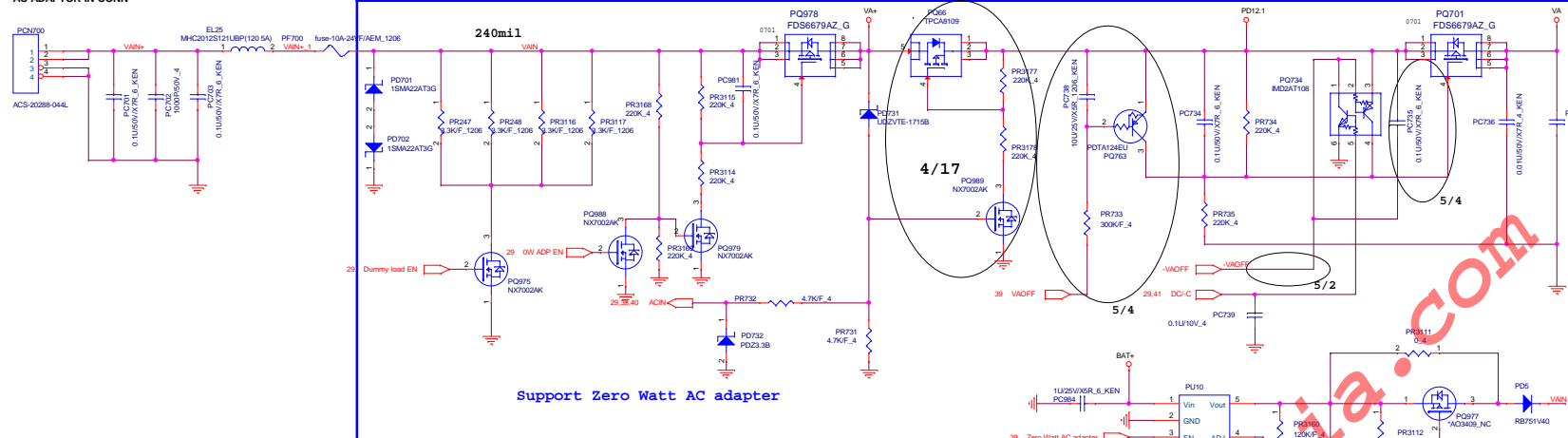
STATE	S3	S5	1.5VSUS	VTTREF	VTT
S0	1	1	on	on	on
S3	0	1	on	on	off
S4/S5	0	0	off	off	off



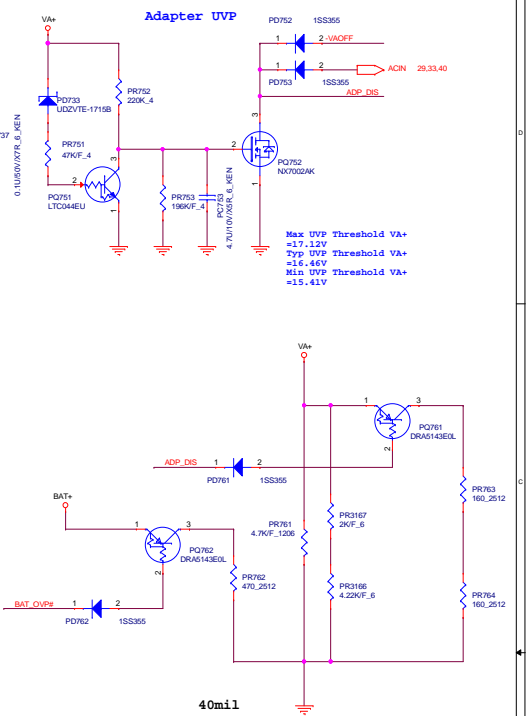
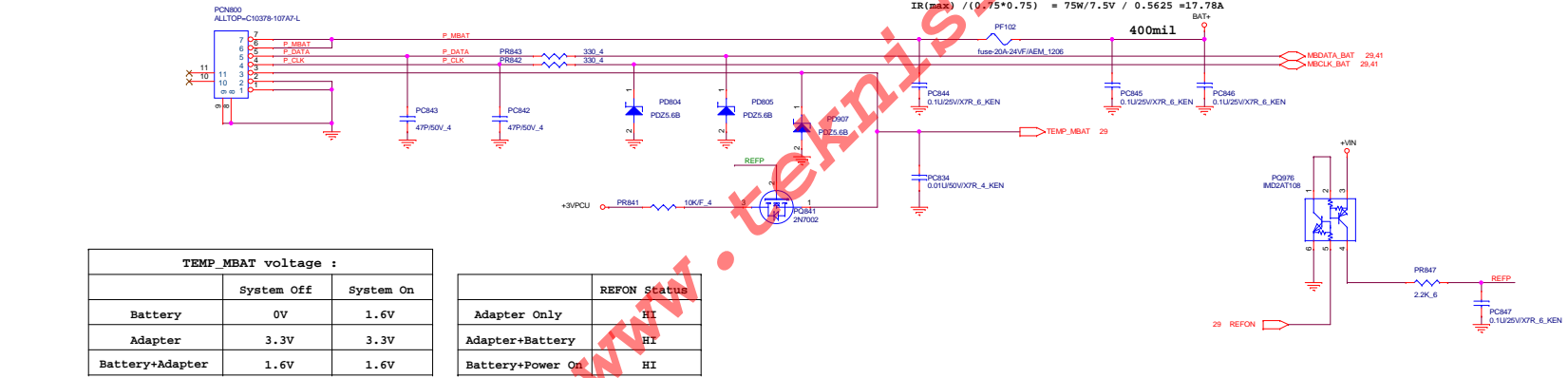




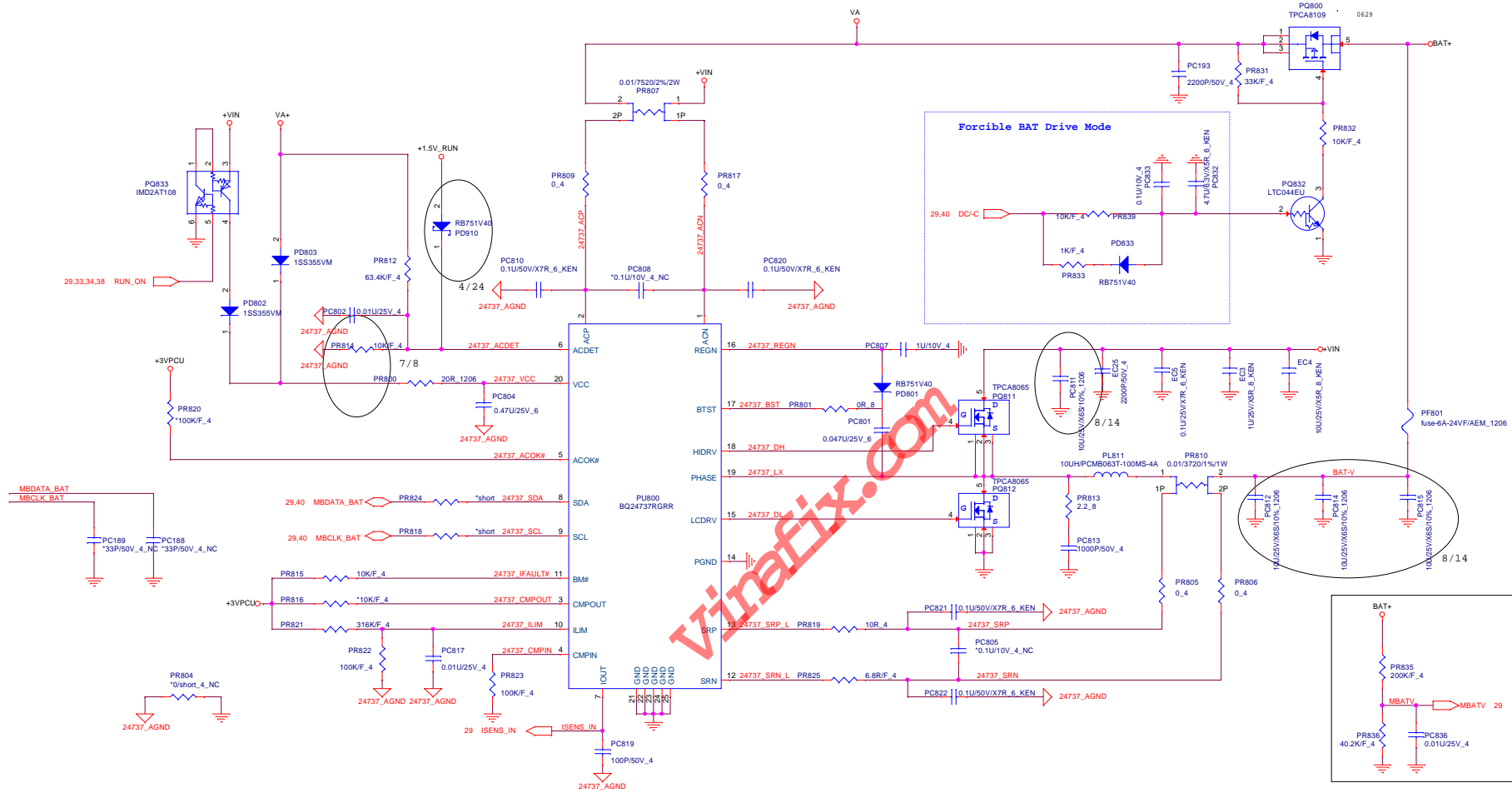
AC ADAPTOR IN CONN

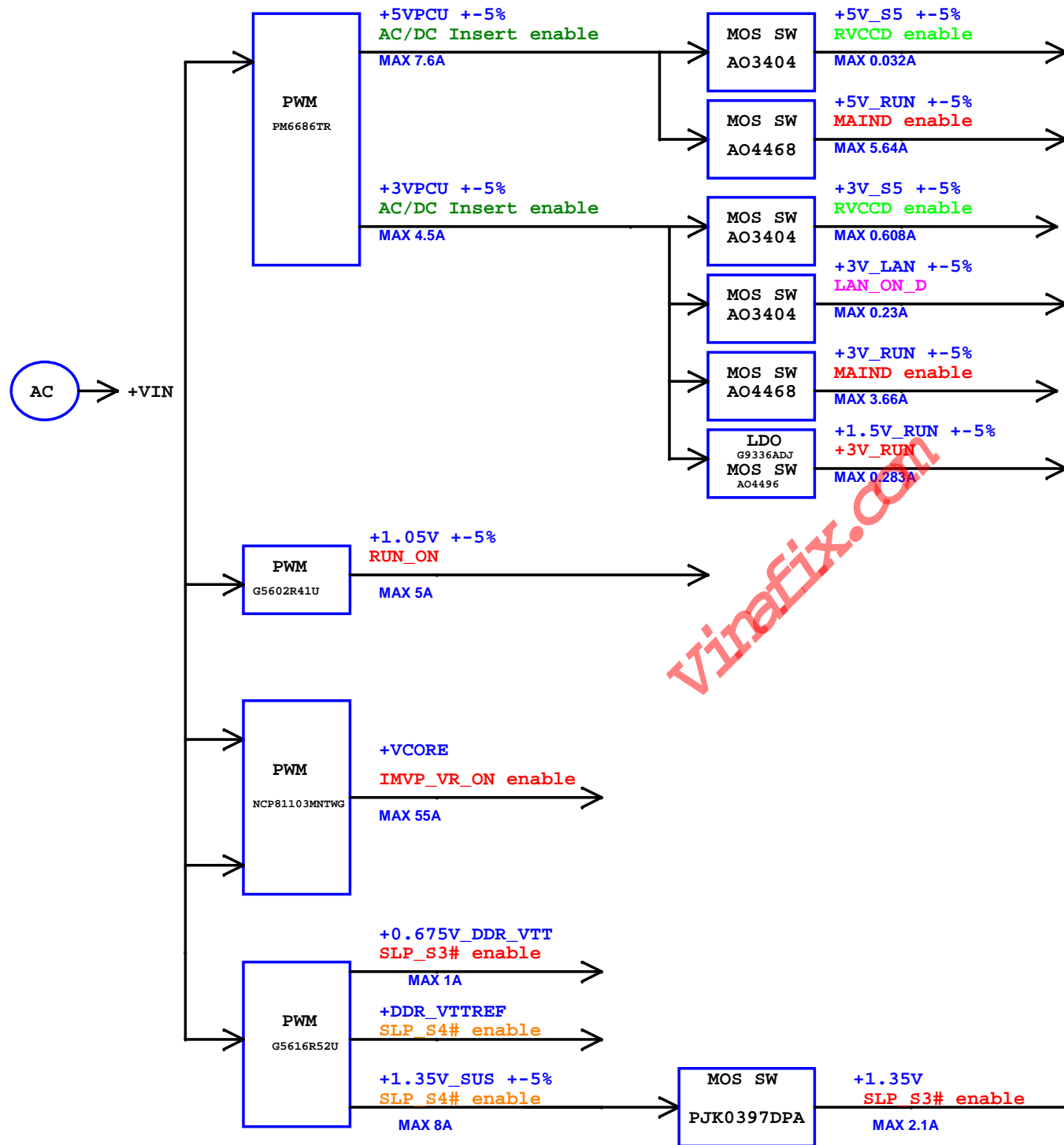


AR1 Battery Connector



41 Battery Charger





RR3A ES2(Rev B).Change List

Date	Changes Summary
2013/04/16	<ol style="list-style-type: none">1. Chang Card solution by 31,32 page2. NFC Driver can't control module in S3, +5V_S5_USB change to +5V_RUN
2013/04/17	<ol style="list-style-type: none">1. Add EC93-EC99 100P/50V by EMI suggest.2. Change from Diode (PD703) to FET. (For Energy Star) Refer to Justice MRT schematic. Del: PD703 Add PQ66, PR3177, PR3178, PQ9893. Adjust the waveform of PLTRST#. Change R446 to 0Ω from 33Ω Change R399 to 51Ω from 0Ω Change R253 to 51Ω from 0Ω4. SYS_PWROK Signal add R655 51ohm in RLTRST#_2 trace5. APWROK Signal for VPRO This signal has a large overshoot. change R626 to 43Ω from 0Ω6. Add series resistor R656 51Ω by SYS_PWROK trace7. VDDQ for DIMMS and CPU follow intel add R657 0Ω on the +15VPCU
2013/04/19	<ol style="list-style-type: none">1. C653-C656 10PF Reserved for EMI2. C11/C14 from 22PF change to 10PF for Crystal fail issue3. Page No.41 Change Battery Charger solution
2013/04/23	<ol style="list-style-type: none">1. Del MR18 10Kohm, link SD_LED# for RTS5227 LED function.2. Del ML1, keep 40mil for RTS5227E vendor confirm3. Del C641, C642 0.1uF, add C657 1000P CLOSE TO CNCARD24. PR900 will change from 8.2Kohm from 20Kohm, power David confirm5. Chang PR88 to 12K ohm from 1Kohm, Adjust the timing for Power Sequence6. add U66:SN74LVC1G17, C660:0.1uF, C659:0.1uF, U67: TC7SH08FU, ME_OFF# Link to PR3176[2], Adjust the timing for Power Sequence7. add U1:SN74LVC1G17, C447:0.1uF, R297:10Kohm, C45:1uF, R122:33ohm, Adjust the timing for Power Sequence.8. Change link INT_HDMI_TXP0 to HDMI_TX2+_R, INT_HDMI_TXN0 to HDMI_TX2-_R INT_HDMI_TXP2 to HDMI_TX0+_R, INT_HDMI_TXN2 to HDMI_TX0-_R follow intel guild line9. Del F20 fuse ES2 stage chang eDP to LVDS solution not need +1.05V power10. JDELCDC1[33] chang link to 2136R_ON net from eDP ED ctrl Panel VCC11. Del R456 0ohm, R457 0ohm, R478 0ohm12. add D27 for LCD VCC ctrl
2013/04/24	<ol style="list-style-type: none">1. add R658, R659 0ohm reserved for ESD2. PR900change from 20k to 10kDelay/latch no function in battery mode3. PR310change from 158K to 150K For OCP4. PR510change from 274K to 249K For OCP5. PR3119change from 174K to 165K For LL6. PR3123 change from 174K to 165K For LL7. PC991 change from 560P to 820P For LL8. PR3149 change from 40.2K to 53.6Kmodify the frequency to reduce mosfet temperatuer9. PC304 change from N/A to 22n delay +3VPCU and +5VPCU enable time10. PR901 change from 1k to 2k For NEC request11. add R658, R659 0ohm reserved for ESD12. Change R446 change to 0Ω for NEC request13. Remove R655 51ohm on the PLTRST#_2 trace.14. Del PLTRST# from JDELCDC1[23] eDP not use it.15. Add C661 1uF on the HWPG-C for NEC request16. unmount R657 0ohm for NEC request
2013/04/25	<ol style="list-style-type: none">1. Change PC304 link from 3V_LX to 3V_DH for mistake2. Change PR3149 from 40.2K to 53.6Kohm3. Change PR415 from 10kohm to 30Kohm for delay +0.675V_DDR_VTT enable time
2013/04/26	<ol style="list-style-type: none">1. Change link PCH_SDI_ROM to U5[5]SI pin for Snoopy san mistake2. Change link PCH_SDO_ROM to U5[2]SO pin for Snoopy san mistake3. Change link EC_SDI_ROM to U10[5]SI pin for Snoopy san mistake4. Change link EC_SDO_ROM to U10[2]SO pin for Snoopy san mistake
2013/04/29	<ol style="list-style-type: none">1. Unmunt C151 : 1000P/50V, MC20 : 220P for NEC request2. D27[1,2]swap pin for design change.
2013/05/01	<ol style="list-style-type: none">1. Add C662 0.1uF_NC, F20_NC fuse link to +5V_USB5 Reserved for NFC/Felica module2. Change PU400 from G5616 to RT8207 for Solve +1.35V_SUS voltage droop when +0.675_DDR_VTT turn on issue3. Change PC735 from 0.1u to 10uFor client request4. change PD853 to PR733:300Kfor client request5. Add C663, C664 0.1uF close to PCH for meet PCI spec6. Add C665, C666 0.1uF close to PCH for meet PCI spec
2013/05/02	<ol style="list-style-type: none">1. Change net name to SYS_PWROK_R from SYS_PWROK2. Add C667 330U meet the FDDG Ver2.0 the Decoupling capacitor spec
2013/05/03	<ol style="list-style-type: none">1. Change PR310 from 150K to 215K form OCP change.2. Add PQ763, PC738, PR377 for protection circuit design change.3. Del TP40, TP67 Reserved SPI Quand mode4. add R660_NC 33ohm, R662_NC 0ohm, PCH_SPI_IO2 link to R6605. add R661_NC 33ohm, R663_NC 0ohm, PCH_SPI_IO2 link to R6616. add R664_NC, R665_NC 30ohm link to PCH_SPI_IO37. Change PQ763 from DRA5143E0L to DRA5124E0L for meet NEC design.
2013/05/03	<ol style="list-style-type: none">1. Current rating for power budget for No.33 page2. Change PL511 from 1.5uto 1u for change choke current rating for power budget3. Change PC735 from 1uFto 0.1uF for NCE request4. Change PR733 from 100kto 300k for NCE request
2013/05/06	<p>Change link EC_SDO link to U10[5]SI</p> <p>Change link EC_SDI link to U10[2]SO</p>

RR3A PP(Rev C).Change List

Date		
2013/05/15	add R666 10k ohm No pop add U68 TC78H08FU BOMVPRO add C668 0.1u BOMVPRO Modify vbro model, VCCASH(PCH) rail falls before APWROK power sequence	
2013/05/31	Change eDP SUSBUS Slave address: 95H Modify LAN VDD009 power description	
2013/06/20	Add R667 10K ohm pull up PCIE_CLKREQ_CARD# for Cardbus design. Change U21 QZ600 P/N from A to A1 for ES2 stage error use. Board ID change R166 from 45.3K ohm to 24.3K ohm Remove R658 10K ohm for RED request. M01 MTS52278 pin9 rename from VREF to RREF mapping pin name.	
2013/06/25	P5 from 1A/32V/POLY/FAST_6 change to FUSE SMD 1.1A 6V POLY KMC38110RY/UL/TUV for NEC AVL parts P7 from 1A/32V/POLY/FAST_6 change to 0.75A/6V/POLY/.8 for NEC AVL parts P8 from 1A/32V/POLY/FAST_6 change to 0.75A/6V/POLY/.8 for NEC AVL parts P9 from 1A/32V/POLY/FAST_6 change to 0.75A/6V/POLY/.8 for NEC AVL parts P10 from 1A/32V/POLY/FAST_6 change to 0.75A/6V/POLY/.8 for NEC AVL parts P11 from 1A/32V/POLY/FAST_6 change to 0.75A/6V/POLY/.8 for NEC AVL parts P13 from 1A/32V/POLY/FAST_6 change to 0.75A/6V/POLY/.8 for NEC AVL parts P14 from 1A/32V/POLY/FAST_6 change to FUSE SMD 1.1A 6V POLY KMC38110RY/UL/TUV for NEC AVL parts P20 from 1A/32V/POLY/FAST_6 change to FUSE SMD 1.1A 6V POLY KMC38110RY/UL/TUV for NEC AVL parts Modify LAN VDD009 power description	
2013/06/26	R426 from 33 ohm change to 0 ohm, AC7 NA for ACX_SDING of Fall time can't meet PCH spec. R80, R86, R99, R141, R152, R161 change from 33 ohm to 47ohm for SPI Duty cycle NA fail fix.	
2013/06/27	Change parts and update PQ978, PQ701, and PQ800 footprint for meet NEC AVL	
2013/06/29	Add PC1021 220u/6.3V cap Reserved for +5VPCU Bounce Add PQ800 Pin 1.2.3 link for mistake	
2013/06/30	Modify PQ800 Pin link for mistake	
2013/07/01	Change PQ978, PQ701 symbol from N-MOS to P-MOS for mistake Change PC1021 220uF/6.3V location close to Q35 5.6.7.8 input pin.	

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RR3A MRT(Rev D).Change List

Date	
2013/07/12	Change Q35 from AO4468 to PD88878 for Bounce issue. Change Q17 from TRANS MOS RJK0397DPA to TRANS MOS TPCA8065-H for EDD
2013/07/8	Change PR814 from 12k to 10k for solve cannot charge issue.
2013/07/18	Change MR12, MR13, MR14,MR15, MR16, MR17 resistor form 43ohm to 33ohm for SD card EA /EMI EA measure.
2013/08/9	R166 from 24.3Kohm cahnge to 12Kohm for MRT Board ID
2013/08/12	1. Add PR765 470 ohm for solve cannot full charge issue 2. Del ECSMB2_CLK_PCU, ECSMB2_DAT_PCU net from EC[67,68PIN]. Del C441,C440,10pF,R106,R107 2.2Kohm, R87 4.7Kohm, R81 4.7Kohm, Q7 2N7002 SMB_RUN_CLK, SMB_RUN_DAT link to JDBL/CBI [11,12PIN] for eDP small board via PCH SMBUS update F/W.
2013/08/15	Change PC1013, PC1014 and PC1016 from CH7331MG808 to CC7390JM201. Change PC811, PC812, PC815, PC814, PC1011, PC1012, PC1005 and PC1006 from CH6104KE202 to CH6104KE204. Change PC1015, C327, C329, C330 to NC. For solve acoustic noise :
2013/08/16	Add PR766 470 ohm NA for solve cannot full charge issue Add ECSMB2_CLK_PCU, ECSMB2_DAT_PCU net from EC[67,68PIN] Add C441,C440,10pF NA, R106,R107 2.2Kohm NA Add Q7 2N7002 NA Add R87,R91 4.7Kohm NA Add Mount R668,R669 0ohm Reserved EC SMBUS Delete PR320, PR450, PR450, PR420, PR3147 0ohm Delete PR19, PR3106, PR3161, PR32, PR53 0.01ohm. Add R134 10kohm

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